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(52) UK CL (Edition L)
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GB 2228380 A GB 2218869 A

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(54) **Phase-locking circuit for swept synthesized source**

(57) In a phase-lock loop for a swept synthesized source in which hysteresis, tuning nonlinearity, and drift over time and temperature of an oscillator 12' incorporated into the swept synthesized source are compensated, the tuning current to the oscillator is initialized to zero to eliminate hysteresis effects. Then, the pretune current is set by 24' to produce the minimum operating frequency of the oscillator. Next, the main phase-lock loop is closed, and a low-frequency synthesizer 16' is swept to in turn sweep the oscillator over a selected frequency span. If the selected frequency span extends over other frequency bands, the oscillator is swept to the maximum frequency of the present band and held at this frequency by a track and hold circuit. The main phase-lock loop is opened, the low-frequency synthesizer is re-initialized, the main phase-lock loop is again closed, and the low-frequency synthesizer is swept again. Each frequency band is crossed in a similar manner until the selected frequency span is swept. In order to improve phase-noise and transient response performance of the low-frequency synthesizer, a phase-lock loop speed-up and stability enhancement circuit comprising a zener diode connected across a passive lag-lead network is incorporated. Pretune calibration for the swept synthesized source is also provided.

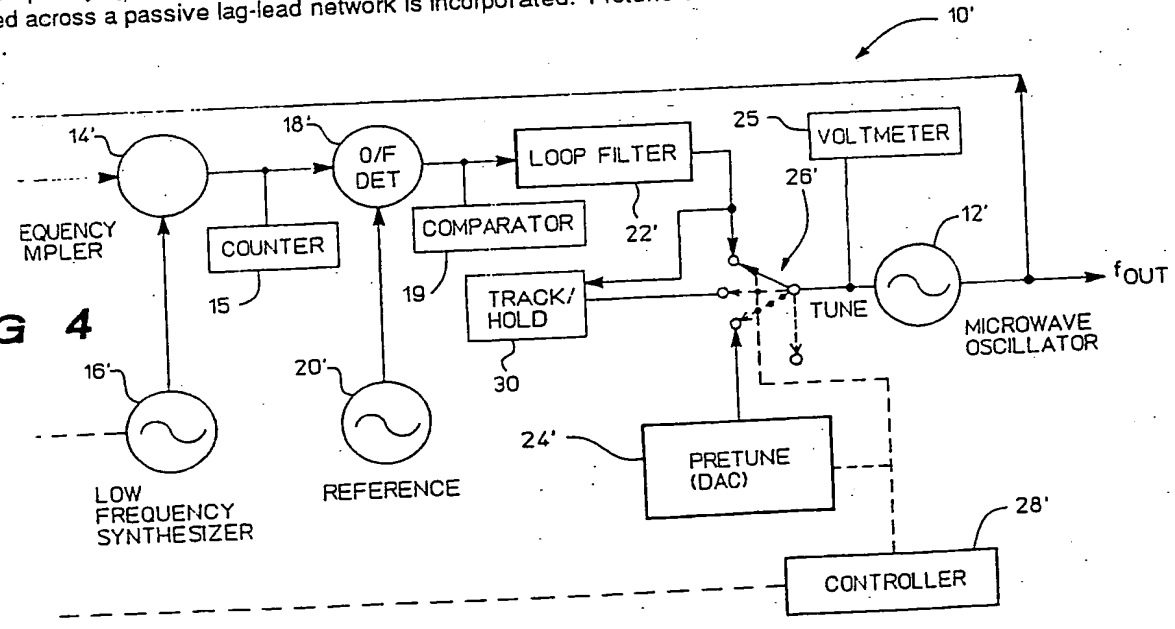


FIG 4

The specification as filed includes a computer program which is not reproduced here; it may be inspected in accordance with Section 118 of the Patents Act 1977

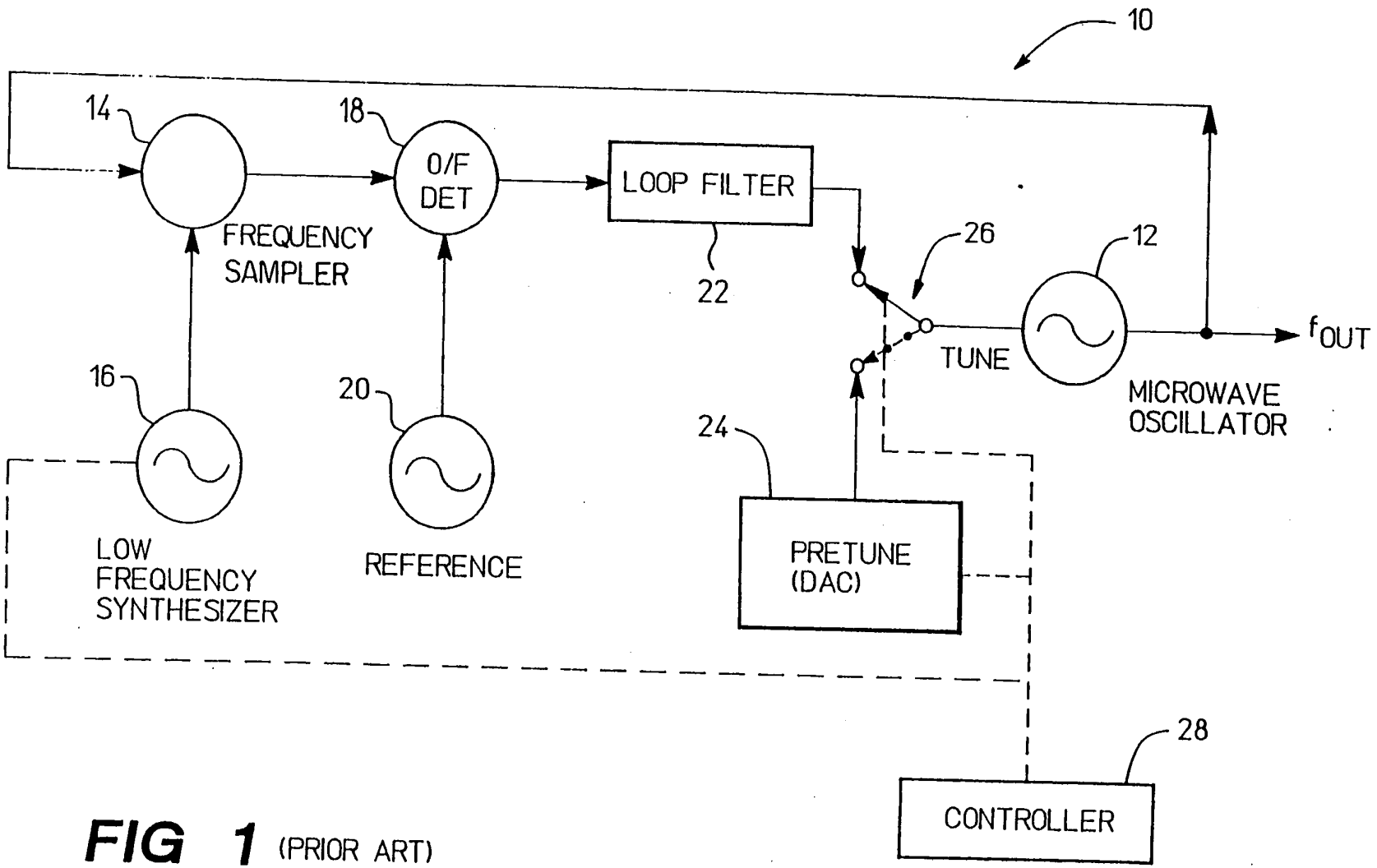


FIG 1 (PRIOR ART)

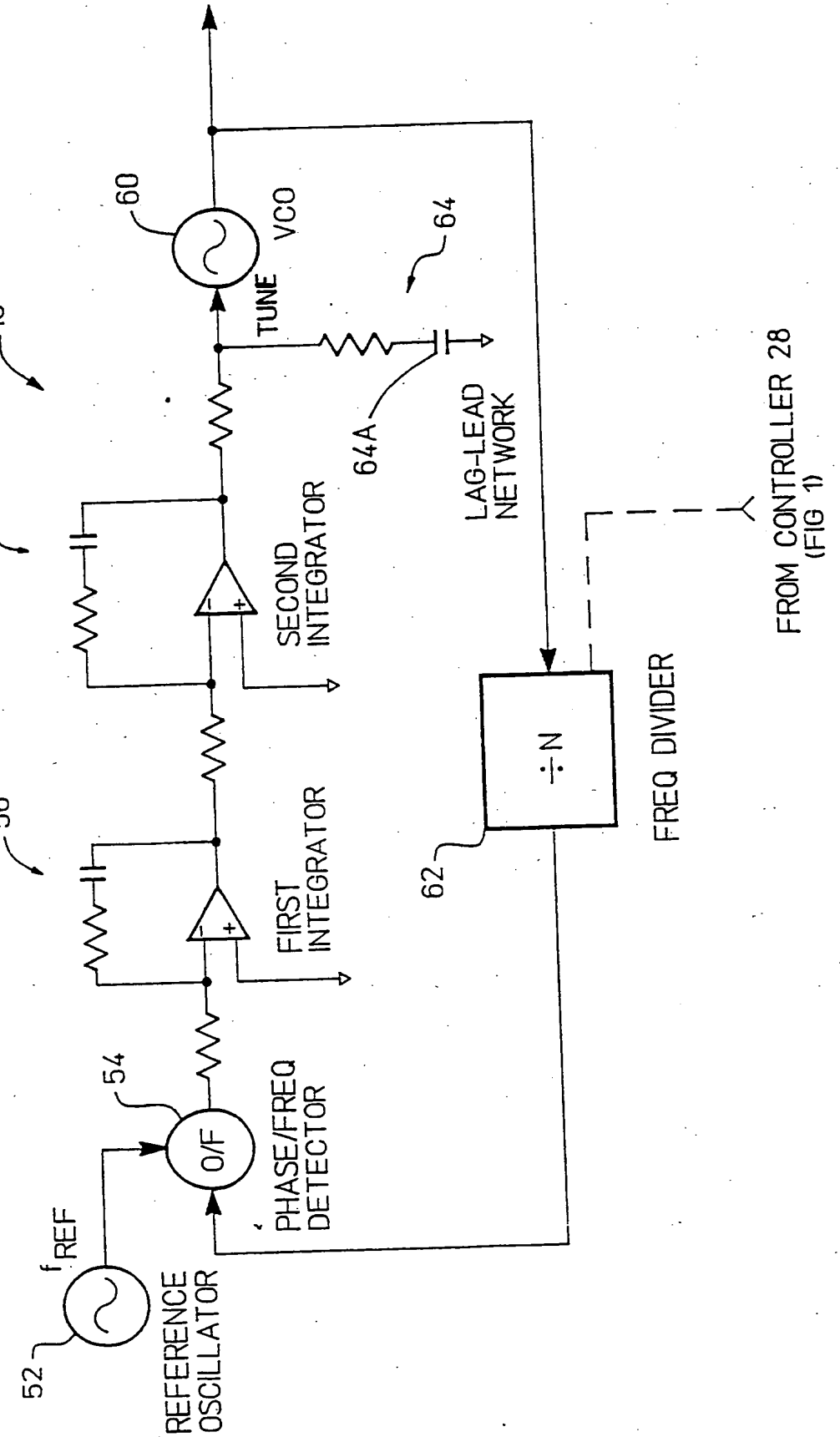


FIG 2 (PRIOR ART)

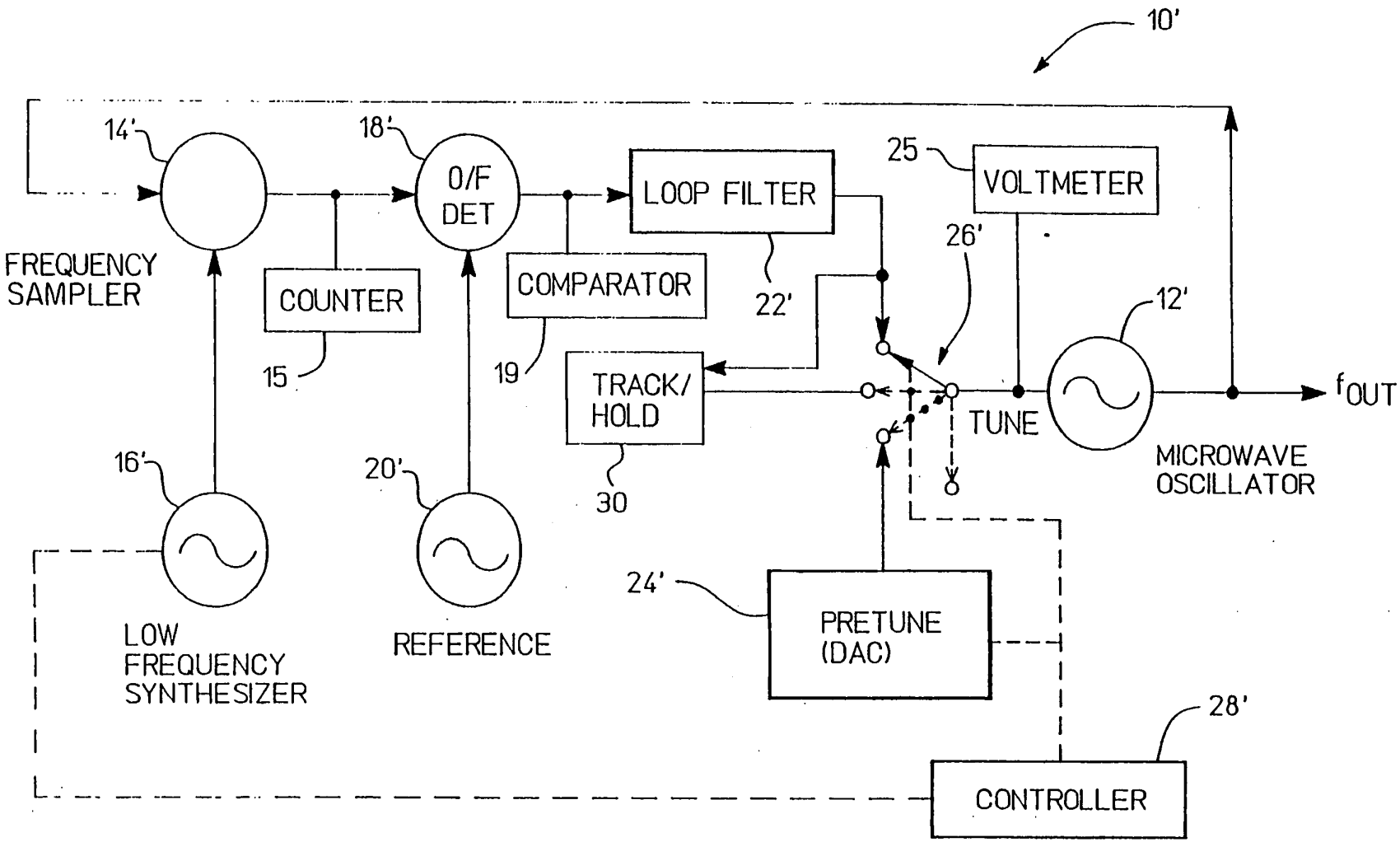

10'
14'
18'
O/F DET
LOOP FILTER
25
VOLTMETER
26'
FREQUENCY SAMPLER
COUNTER
15
COMPARATOR
19
22'
12'
TRACK/ HOLD
30
TUNE
f_{OUT}
MICROWAVE OSCILLATOR
16'
20'
24'
PRETUNE (DAC)
LOW FREQUENCY SYNTHESIZER
REFERENCE
28'
CONTROLLER

FIG 4

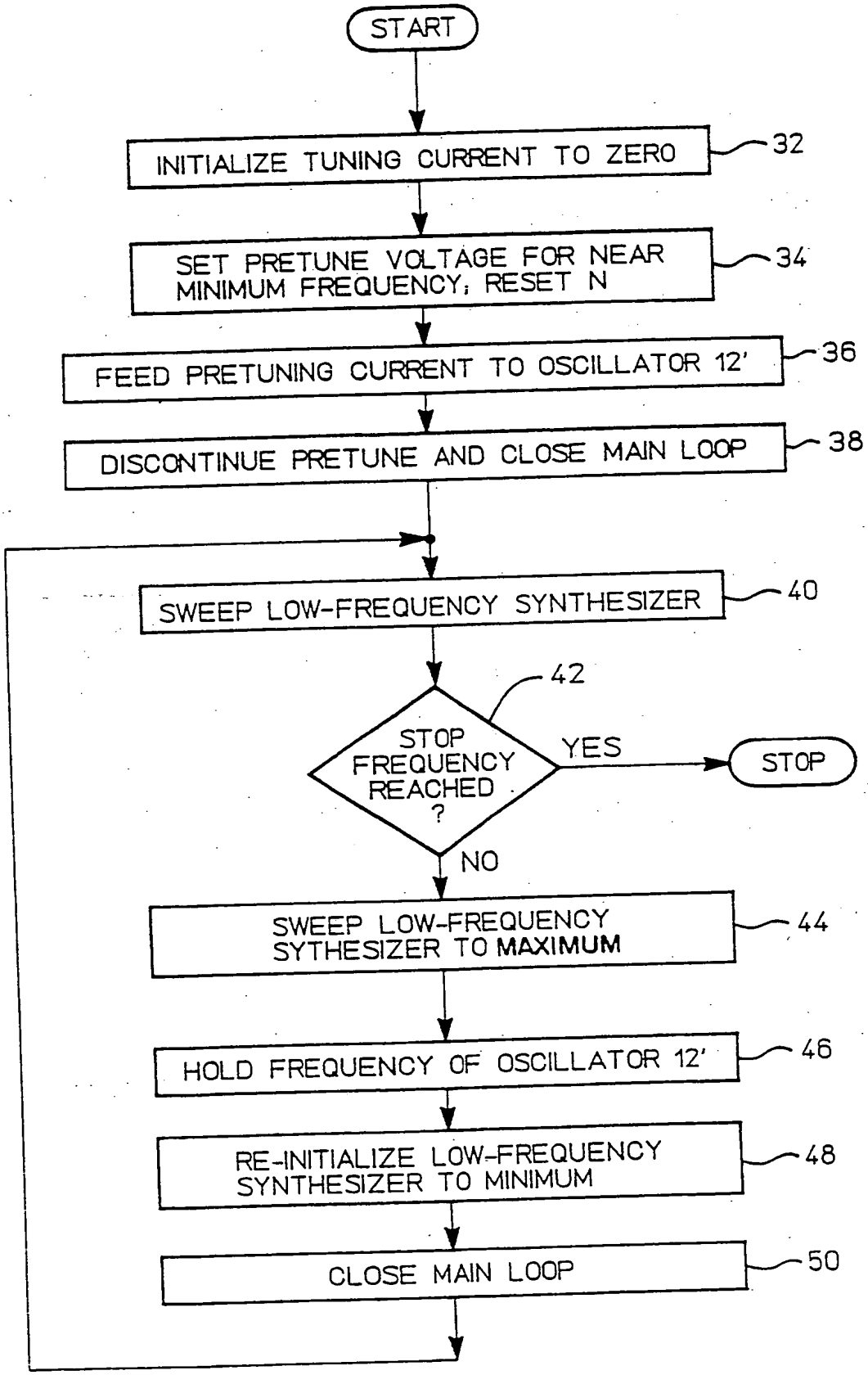

START
INITIALIZE TUNING CURRENT TO ZERO
32
SET PRETUNE VOLTAGE FOR NEAR MINIMUM FREQUENCY; RESET N
34
FEED PRETUNING CURRENT TO OSCILLATOR 12'
36
DISCONTINUE PRETUNE AND CLOSE MAIN LOOP
38
SWEEP LOW-FREQUENCY SYNTHESIZER
40
42
STOP FREQUENCY REACHED ?
YES
STOP
NO
SWEEP LOW-FREQUENCY SYTHESIZER TO MAXIMUM
44
HOLD FREQUENCY OF OSCILLATOR 12'
46
RE-INITIALIZE LOW-FREQUENCY SYNTHESIZER TO MINIMUM
48
CLOSE MAIN LOOP
50

FIG 5

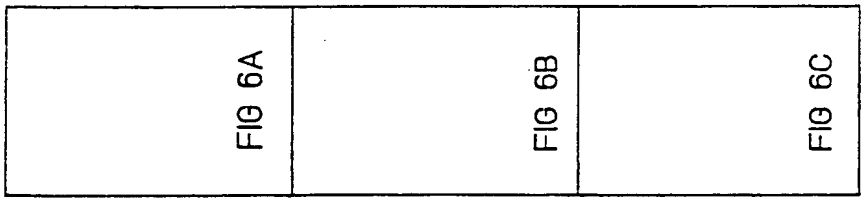


FIG 6

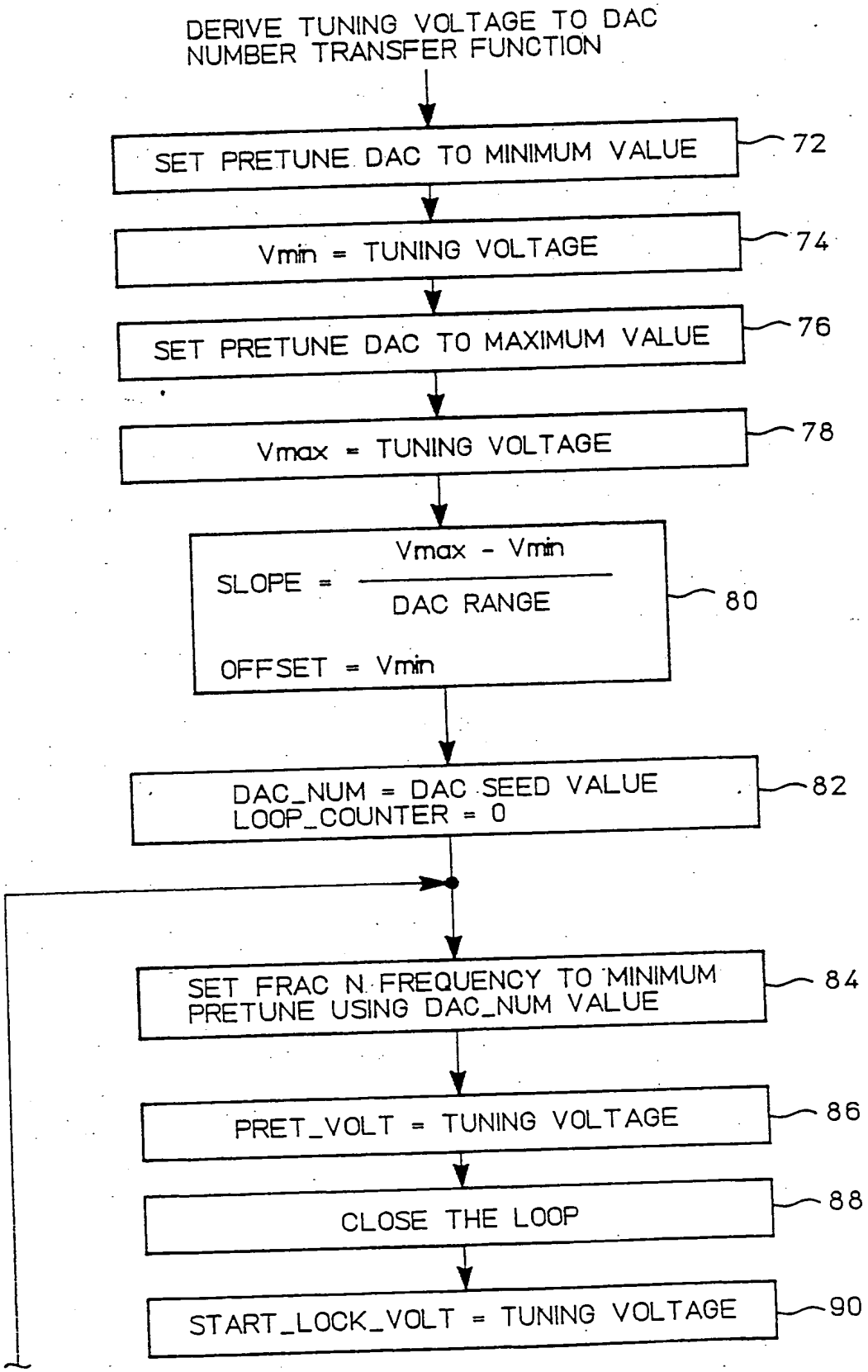

DERIVE TUNING VOLTAGE TO DAC NUMBER TRANSFER FUNCTION
SET PRETUNE DAC TO MINIMUM VALUE
72
Vmin = TUNING VOLTAGE
74
SET PRETUNE DAC TO MAXIMUM VALUE
76
Vmax = TUNING VOLTAGE
78
SLOPE = Vmax - Vmin / DAC RANGE
OFFSET = Vmin
80
DAC_NUM = DAC SEED VALUE
LOOP_COUNTER = 0
82
SET FRAC N FREQUENCY TO MINIMUM PRETUNE USING DAC_NUM VALUE
84
PRET_VOLT = TUNING VOLTAGE
86
CLOSE THE LOOP
88
START_LOCK_VOLT = TUNING VOLTAGE
90

FIG 6A

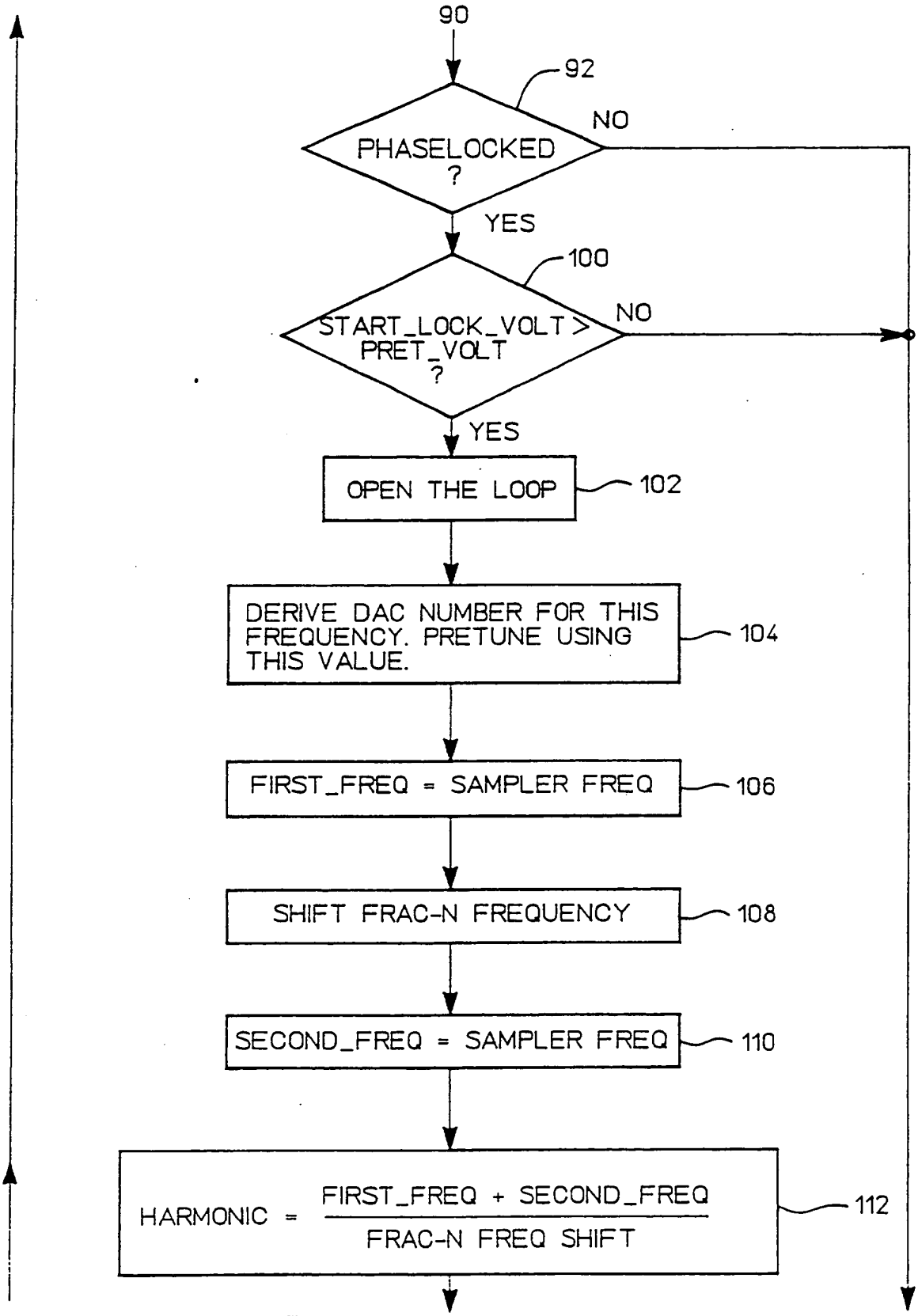

90
92
PHASELOCKED ?
NO
YES
100
START_LOCK_VOLT > PRET_VOLT ?
NO
YES
OPEN THE LOOP
102
DERIVE DAC NUMBER FOR THIS FREQUENCY. PRETUNE USING THIS VALUE.
104
FIRST_FREQ = SAMPLER FREQ
106
SHIFT FRAC-N FREQUENCY
108
SECOND_FREQ = SAMPLER FREQ
110
HARMONIC = FIRST_FREQ + SECOND_FREQ / FRAC-N FREQ SHIFT
112
114

FIG 6B

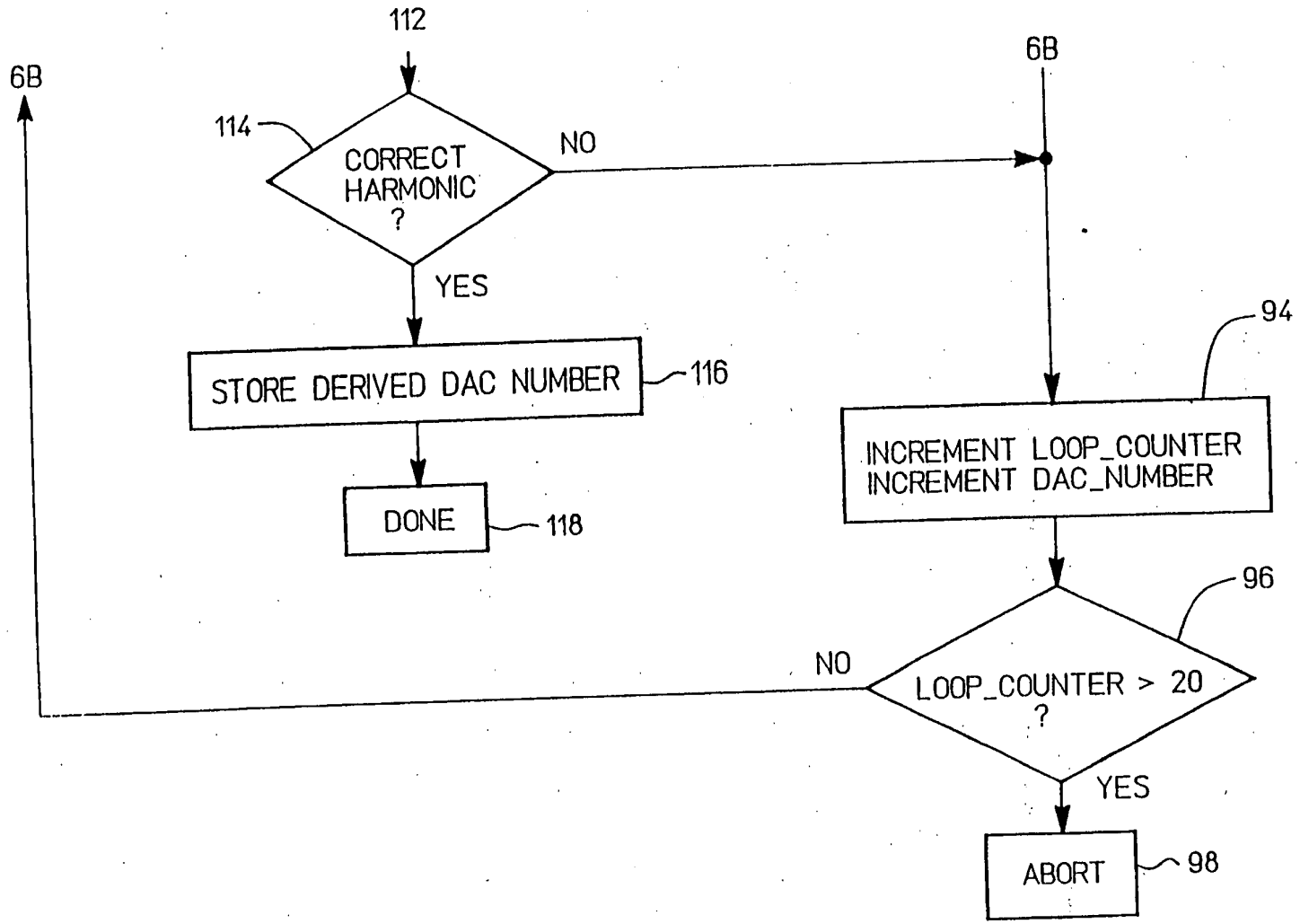

112
6B
6B
114
CORRECT HARMONIC ?
NO
YES
STORE DERIVED DAC NUMBER
116
DONE
118
94
INCREMENT LOOP_COUNTER
INCREMENT DAC_NUMBER
96
NO
LOOP_COUNTER > 20 ?
YES
ABORT
98

FIG 6C

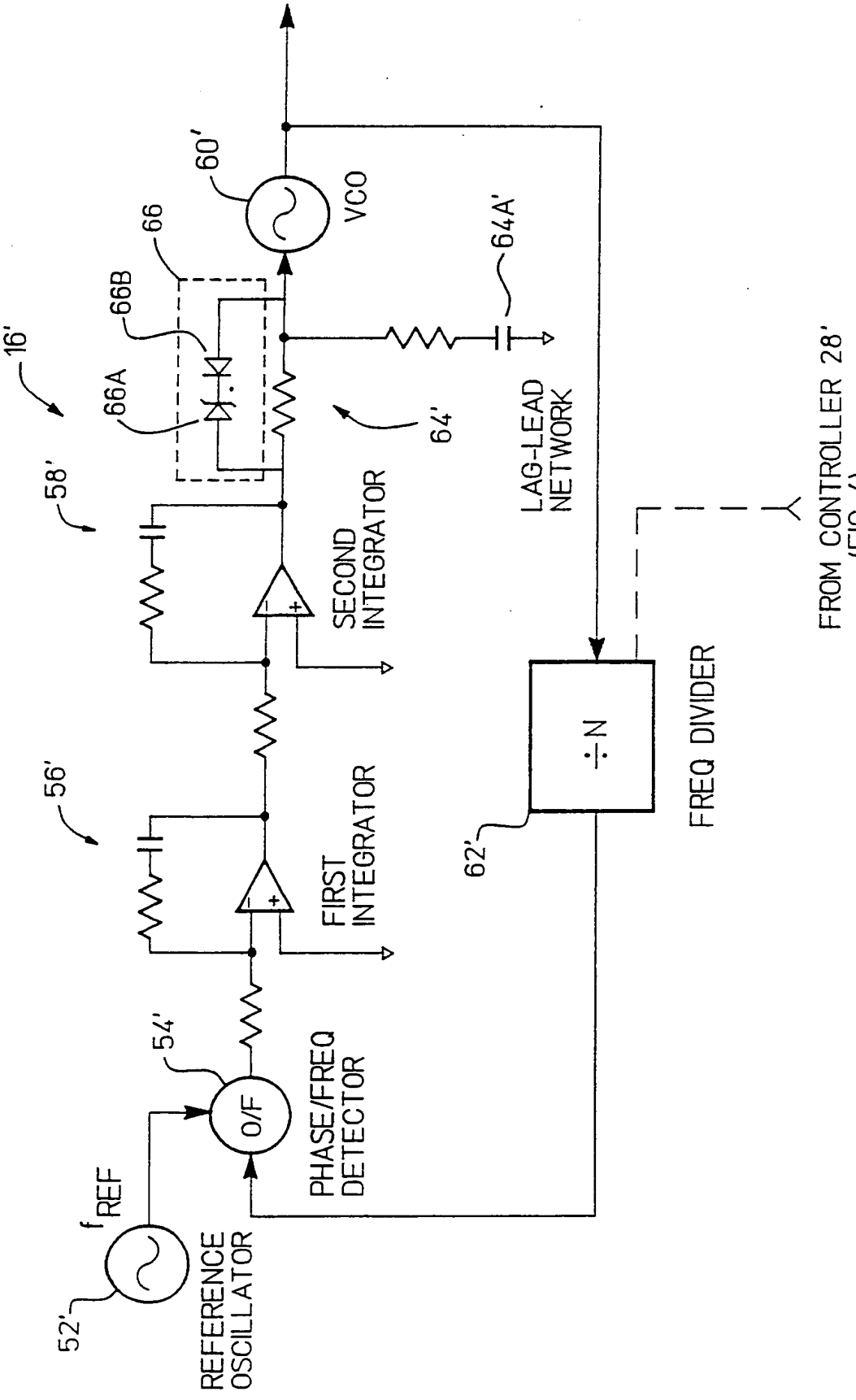
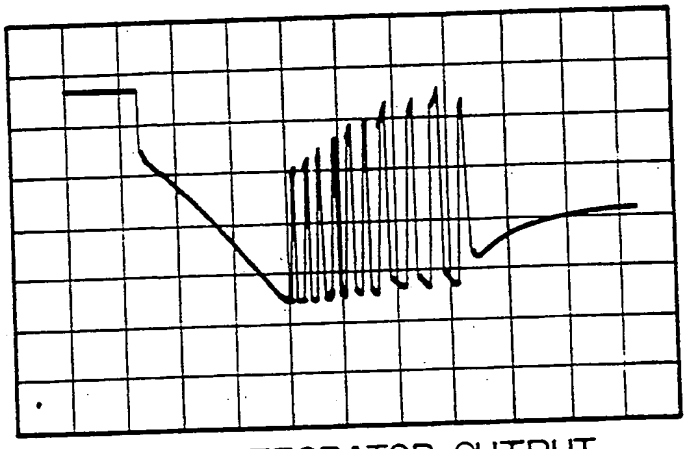
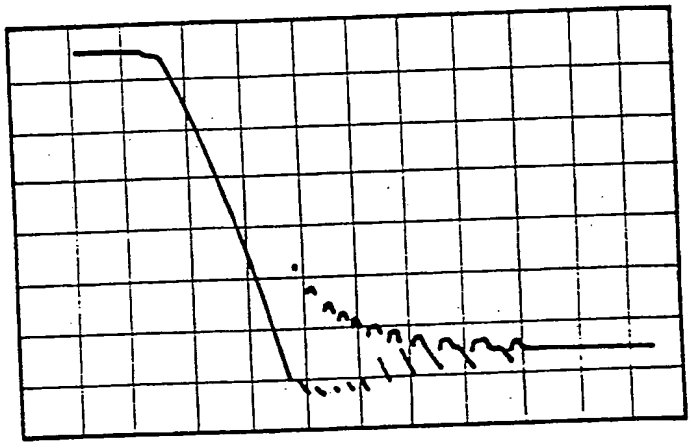

16'
58'
56'
66
66B
66A
60'
VCO
64A'
64'
LAG-LEAD NETWORK
SECOND INTEGRATOR
FIRST INTEGRATOR
÷N
62'
FREQ DIVIDER
FROM CONTROLLER 28' (FIG 4)
54'
O/F
PHASE/FREQ DETECTOR
f_{REF}
52'
REFERENCE OSCILLATOR

FIG 7



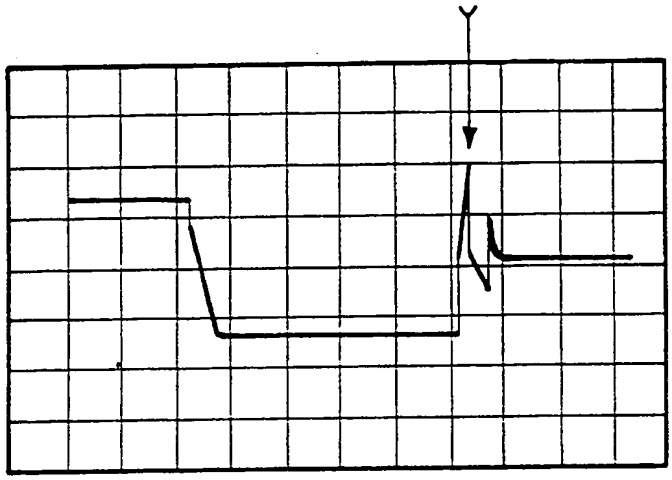
SECOND INTEGRATOR OUTPUT
W/ CIRCUIT 66
5V/DIV, 200μs/DIV

FIG 8A



VCO TUNE VOLTAGE
W/ CIRCUIT 66
2V/DIV, 200μs/DIV

FIG 8B



SECOND INTEGRATOR OUTPUT
10V/DIV, 1ms/DIV

FIG 3 (PRIOR ART)

LAG-LEAD CAPACITOR VOLTAGE
W/ CIRCUIT 66
2V/DIV, 200 μs/DIV

FIG 8C

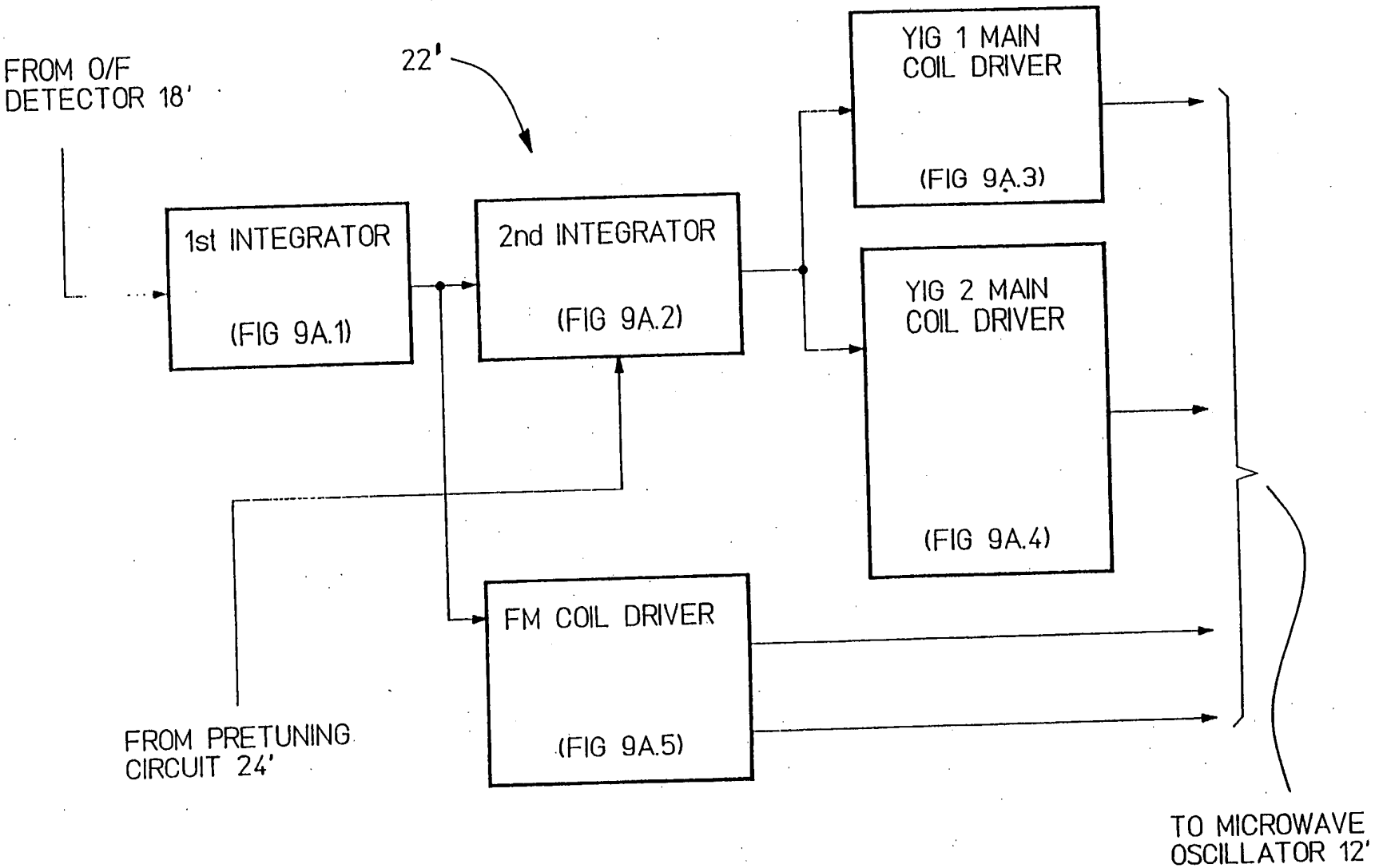

FROM O/F
DETECTOR 18'
22'
1st INTEGRATOR
(FIG 9A.1)
2nd INTEGRATOR
(FIG 9A.2)
YIG 1 MAIN
COIL DRIVER
(FIG 9A.3)
YIG 2 MAIN
COIL DRIVER
(FIG 9A.4)
FM COIL DRIVER
(FIG 9A.5)
FROM PRETUNING
CIRCUIT 24'
TO MICROWAVE
OSCILLATOR 12'

FIG 9A

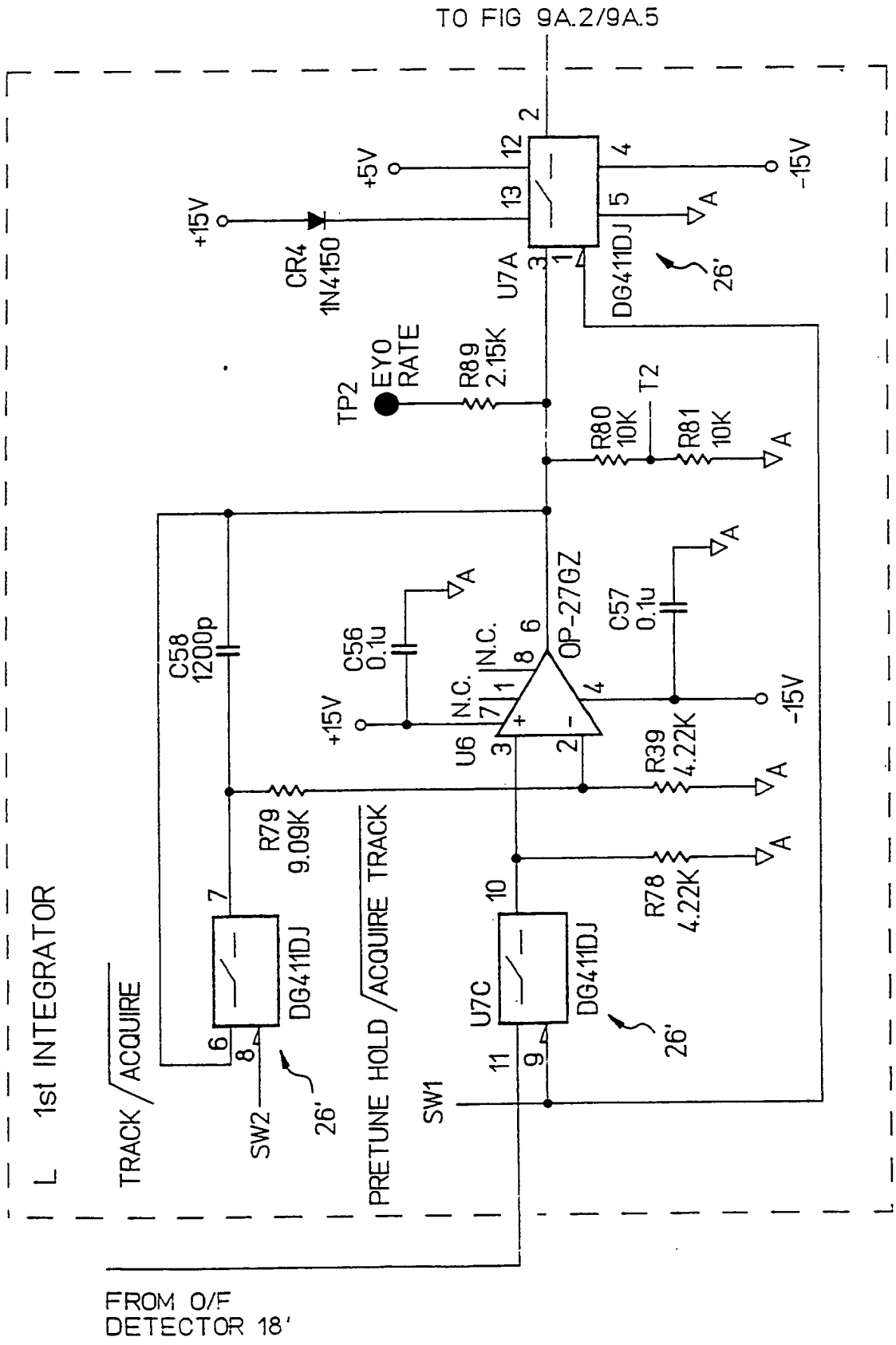

TO FIG 9A.2/9A.5
L 1st INTEGRATOR
TRACK /ACQUIRE
PRETUNE HOLD /ACQUIRE TRACK
+15V
+5V
-15V
CR4
1N4150
U7A
DG411DJ
26'
TP2
EYO
RATE
R89
2.15K
R80
10K
T2
R81
10K
C58
1200p
C56
0.1u
C57
0.1u
N.C.
OP-27GZ
U6
R39
4.22K
R79
9.09K
R78
4.22K
U7C
SW1
SW2
FROM O/F
DETECTOR 18'

FIG 9A.1

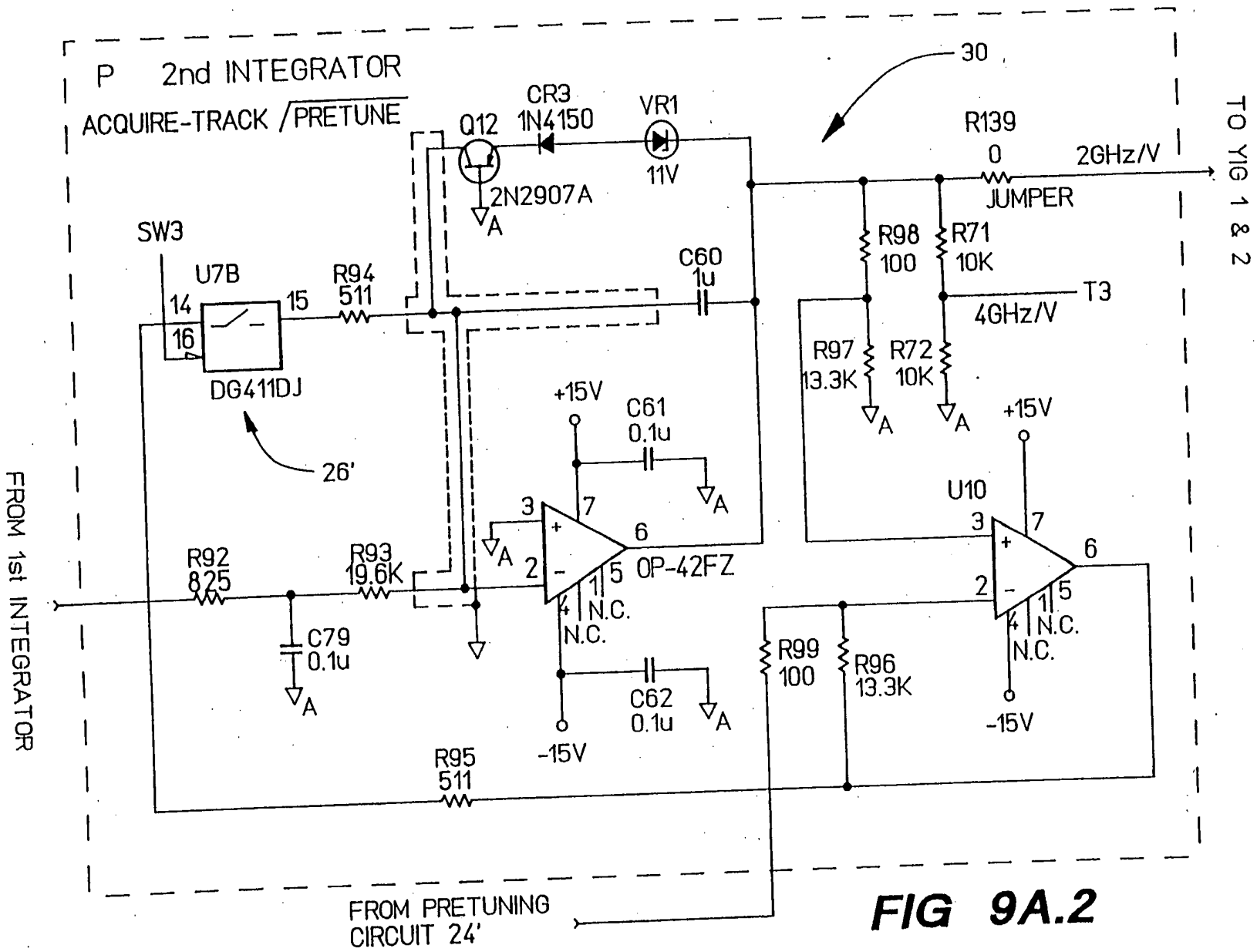

P 2nd INTEGRATOR
ACQUIRE-TRACK /PRETUNE
30
CR3
1N4150
VR1
11V
Q12
2N2907A
R139
0
JUMPER
2GHz/V
TO YIG 1 & 2
SW3
U7B
14
15
16
DG411DJ
R94
511
C60
1u
R98
100
R71
10K
T3
4GHz/V
R97
13.3K
R72
10K
26'
+15V
C61
0.1u
U10
R92
825
R93
19.6K
OP-42FZ
N.C.
C79
0.1u
C62
0.1u
-15V
R99
100
R96
13.3K
R95
511
FROM 1st INTEGRATOR
FROM PRETUNING
CIRCUIT 24'

FIG 9A.2

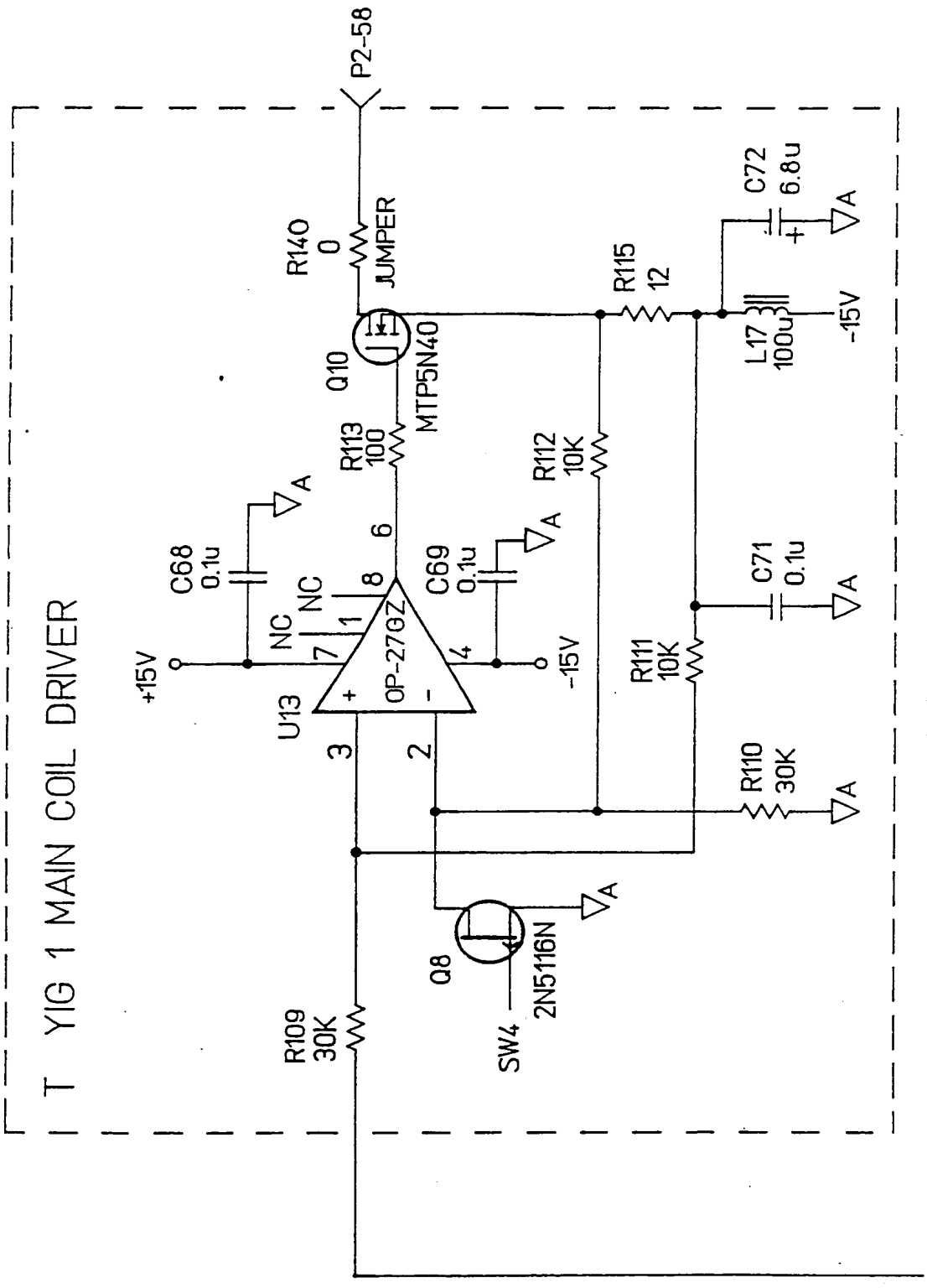

T YIG 1 MAIN COIL DRIVER
P2-58
R140
0
JUMPER
Q10
MTP5N40
R113
100
R112
10K
R115
12
C72
6.8u
L17
100u
-15V
C68
0.1u
C69
0.1u
C71
0.1u
+15V
NC
NC
U13
OP-270Z
R111
10K
R110
30K
R109
30K
Q8
2N5116N
SW4
A

FIG 9A.3

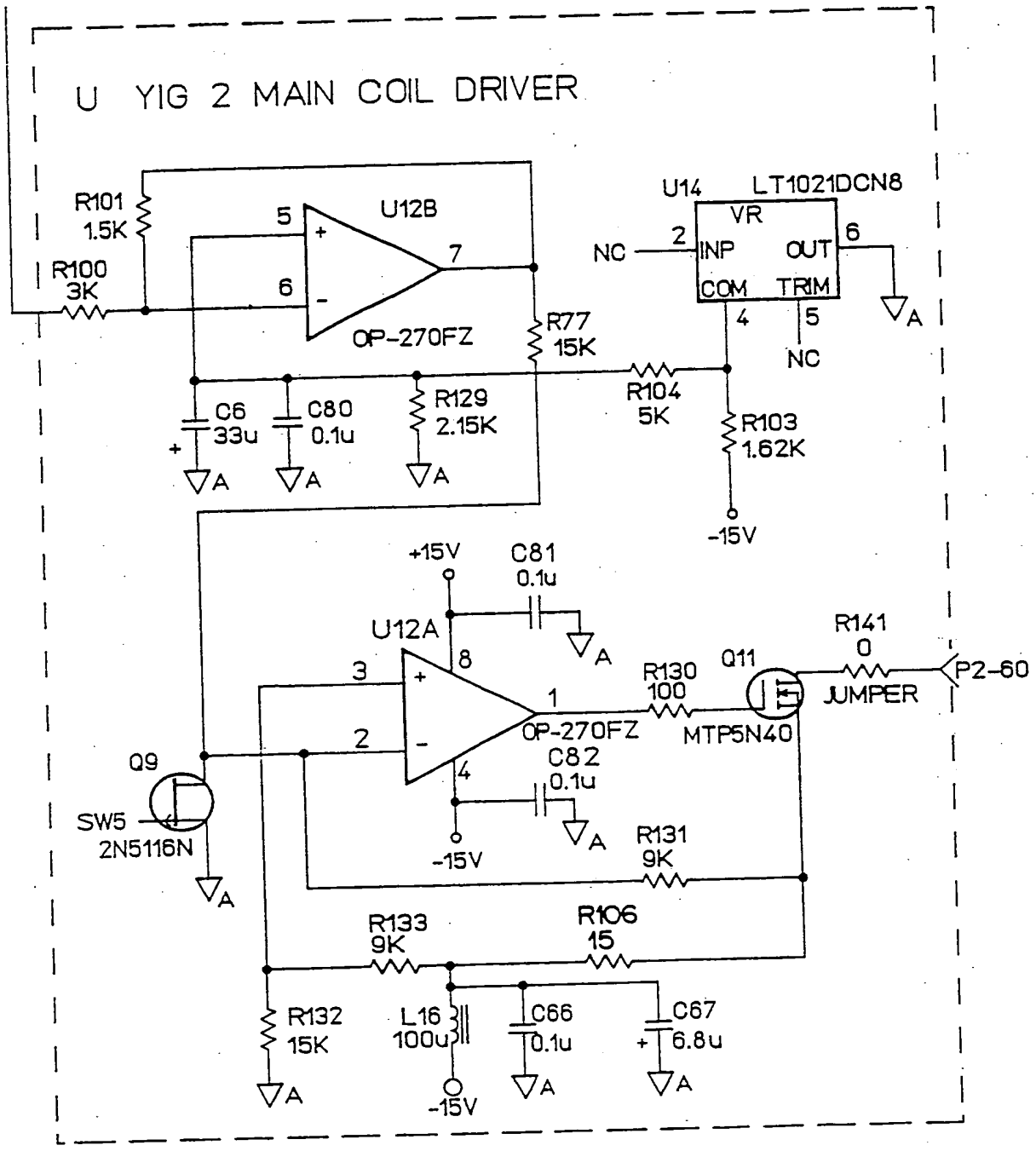

U YIG 2 MAIN COIL DRIVER
R101
1.5K
R100
3K
U12B
OP-270FZ
R77
15K
U14
LT1021DCN8
VR
NC
INP
OUT
COM
TRIM
NC
C6
33u
C80
0.1u
R129
2.15K
R104
5K
R103
1.62K
-15V
+15V
C81
0.1u
U12A
R130
100
Q11
MTP5N40
R141
0
JUMPER
P2-60
OP-270FZ
C82
0.1u
Q9
SW5
2N5116N
R131
9K
R133
9K
R106
15
R132
15K
L16
100u
C66
0.1u
C67
6.8u
A

FIG 9A.4

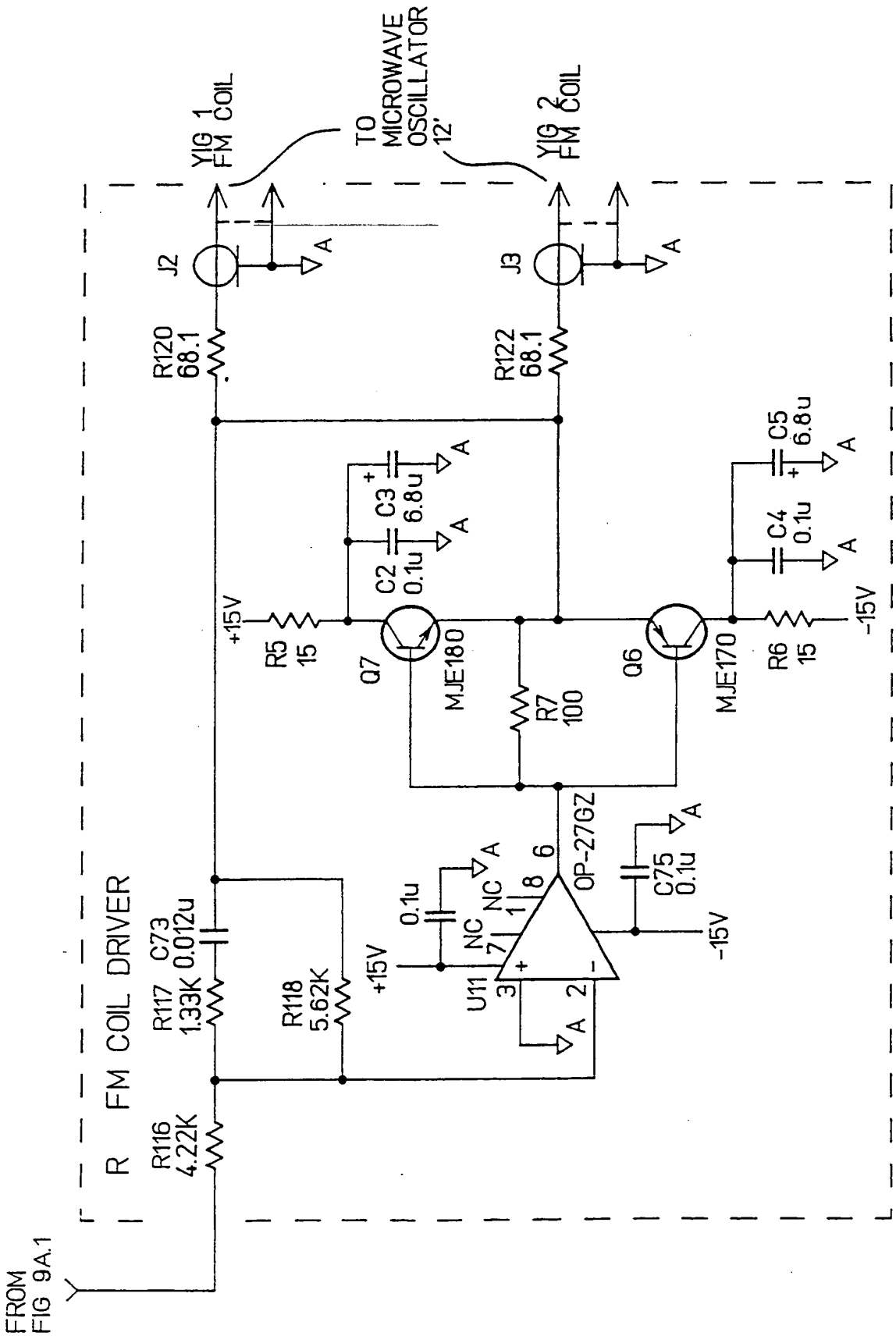

FROM FIG 9A.1
R FM COIL DRIVER
R116 4.22K
R117 1.33K
C73 0.012u
R118 5.62K
+15V
0.1u
NC
NC
U11
OP-27GZ
C75 0.1u
-15V
R5 15
Q7 MJE180
R7 100
Q6 MJE170
R6 15
C2 0.1u
C3 6.8u
C4 0.1u
C5 6.8u
R120 68.1
R122 68.1
J2
J3
YIG 1 FM COIL
YIG 2 FM COIL
TO MICROWAVE OSCILLATOR 12'
A

FIG 9A.5

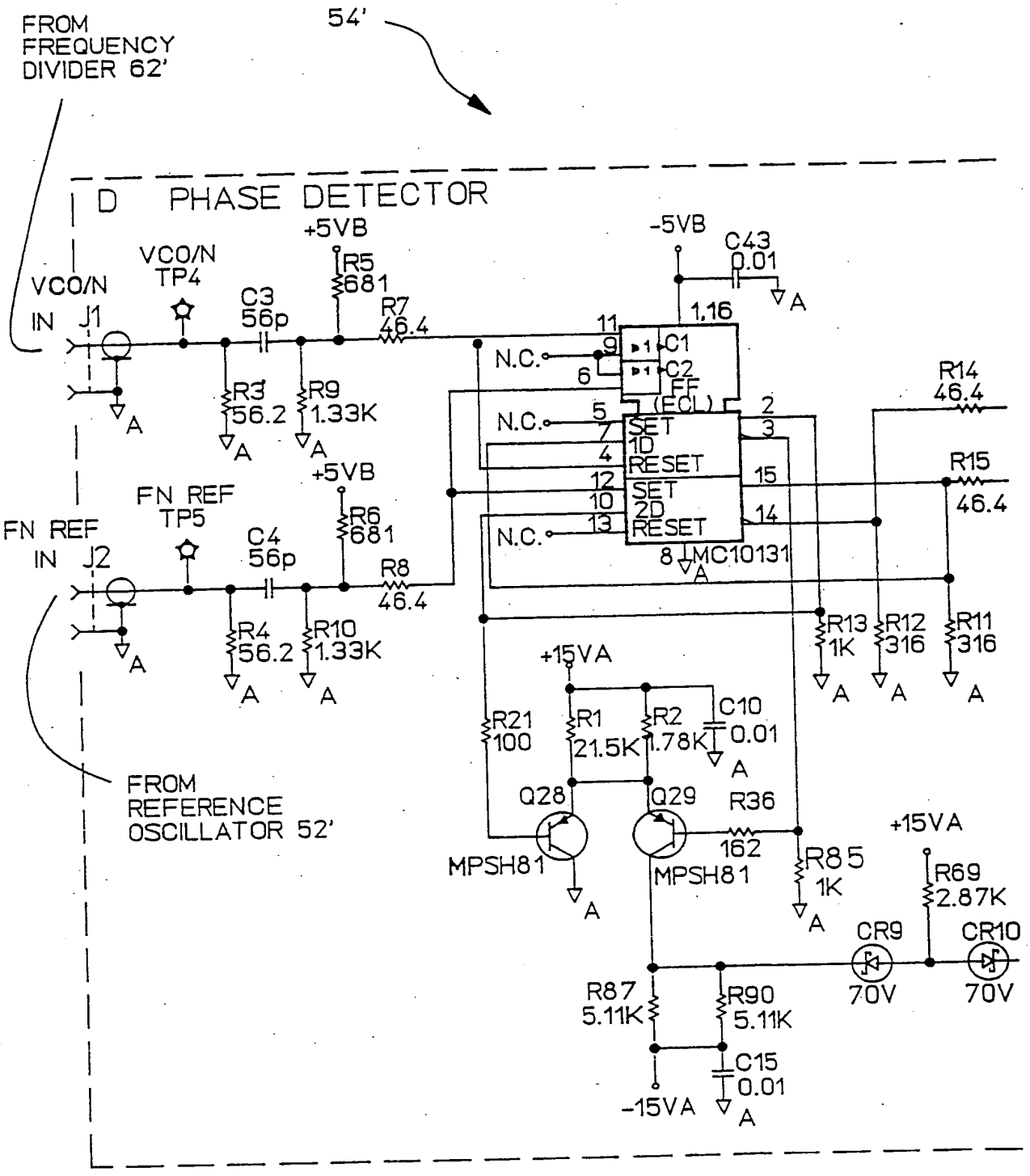

FROM
FREQUENCY
DIVIDER 62'
54'
D PHASE DETECTOR
+5VB
-5VB
C43
0.01
VCO/N
IN J1
VCO/N
TP4
C3
56p
R5
681
R7
46.4
1.16
11
9
6
N.C.
C1
C2
FF
(ECL)
R3
56.2
R9
1.33K
N.C.
5
7
4
12
10
13
SET
1D
RESET
SET
2D
RESET
2
3
15
14
8
MC10131
R14
46.4
R15
46.4
FN REF
IN J2
FN REF
TP5
C4
56p
R6
681
R8
46.4
R4
56.2
R10
1.33K
R13
1K
R12
316
R11
316
+15VA
R21
100
R1
21.5K
R2
1.78K
C10
0.01
Q28
Q29
R36
162
MPSH81
MPSH81
R85
1K
+15VA
R69
2.87K
CR9
CR10
70V
70V
R87
5.11K
R90
5.11K
C15
0.01
-15VA
FROM
REFERENCE
OSCILLATOR 52'

FIG 9B.1

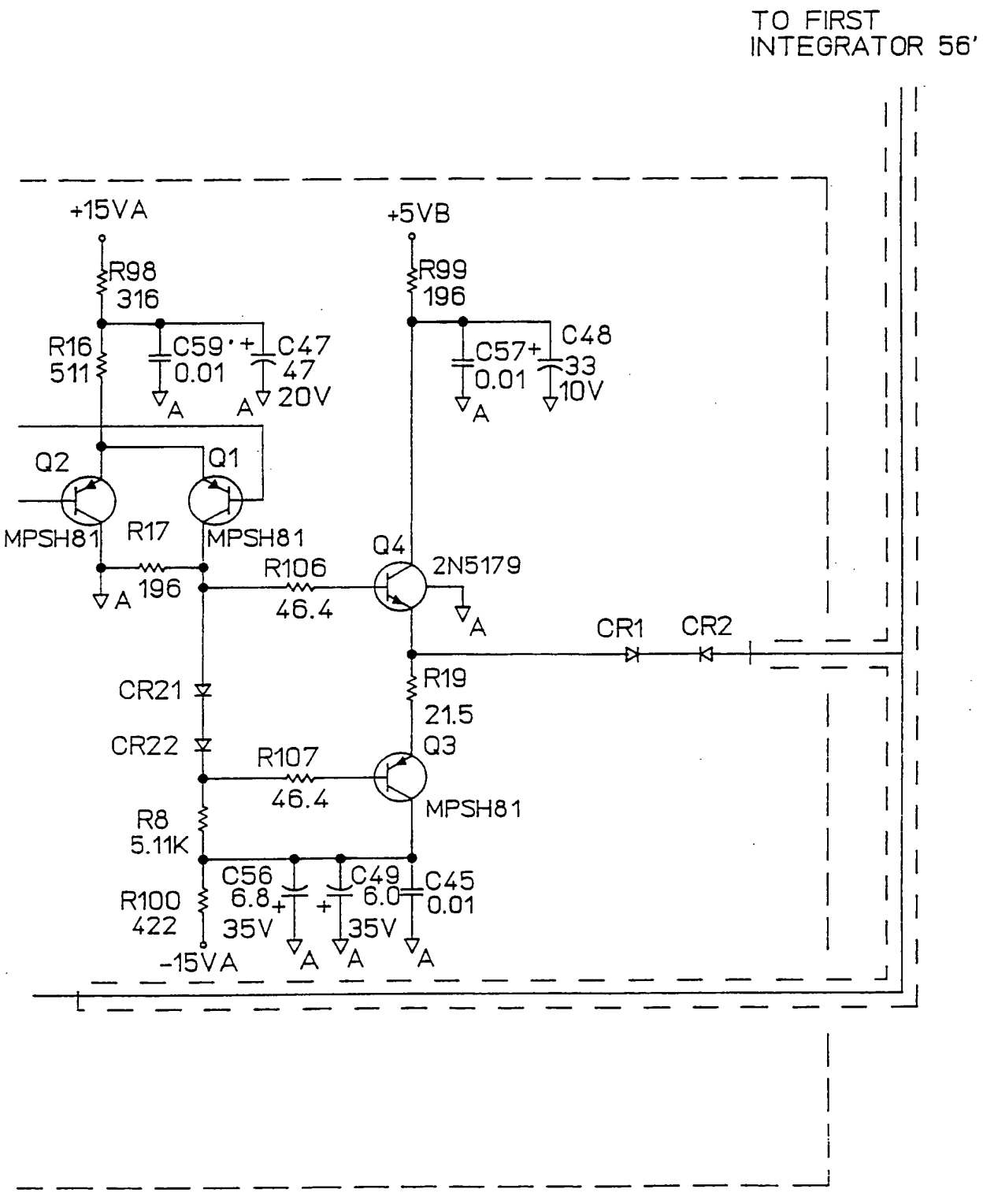

TO FIRST
INTEGRATOR 56'
+15VA
+5VB
R98
316
R99
196
R16
511
C59
0.01
C47
47
20V
C57
0.01
C48
33
10V
A
Q2
Q1
MPSH81
R17
MPSH81
196
R106
46.4
Q4
2N5179
CR1
CR2
CR21
CR22
R19
21.5
R107
46.4
Q3
MPSH81
R8
5.11K
R100
422
C56
6.8
35V
C49
6.0
35V
C45
0.01
-15VA

FIG 9B.2

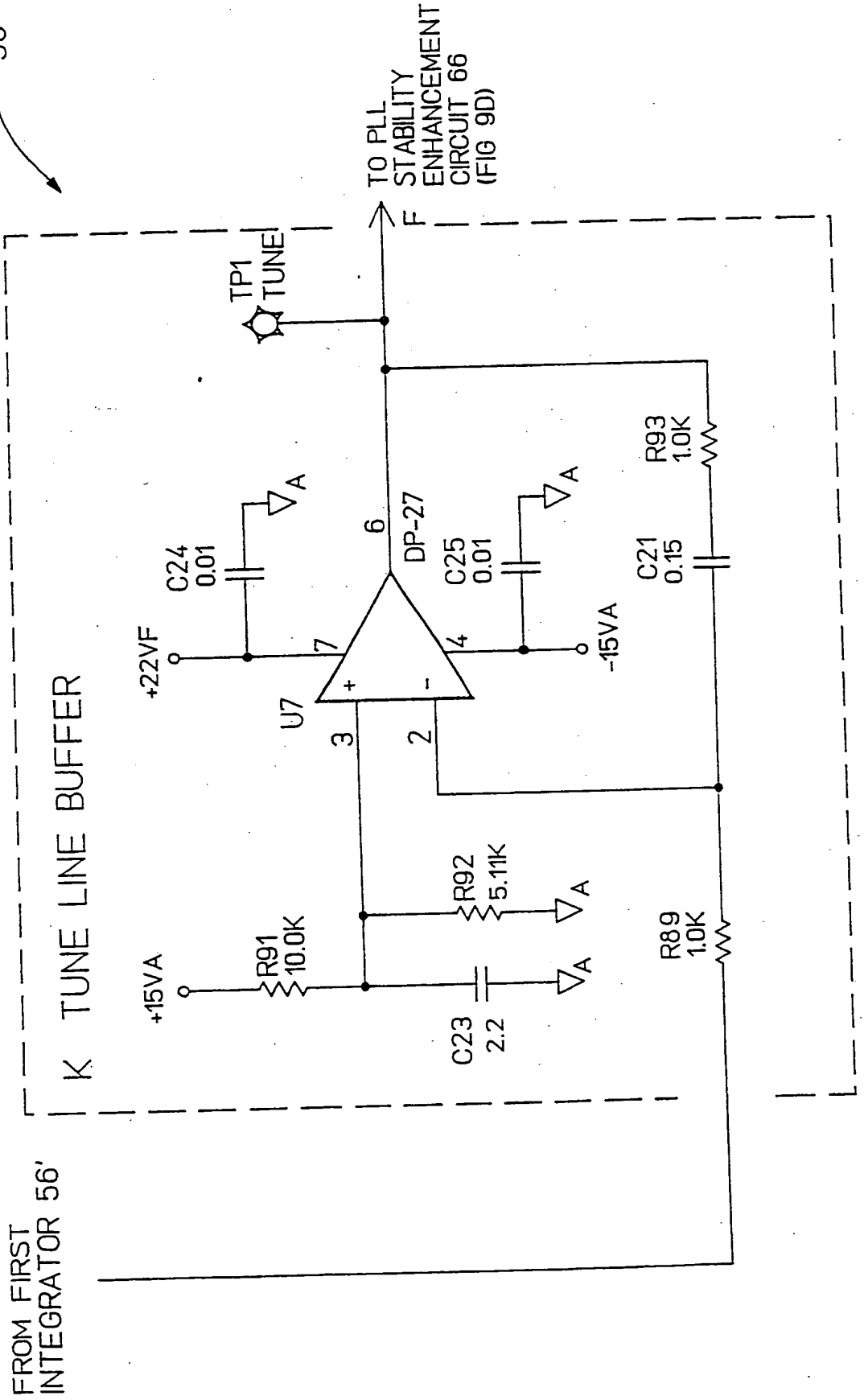

58'
TO PLL STABILITY ENHANCEMENT CIRCUIT 66 (FIG 9D)
F
K TUNE LINE BUFFER
TP1 TUNE
C24 0.01
C25 0.01
C21 0.15
R93 1.0K
R92 5.11K
R91 10.0K
R89 1.0K
C23 2.2
+22VF
+15VA
-15VA
U7
DP-27
6
7
4
3
2
+
-
FROM FIRST INTEGRATOR 56'

FIG 9C

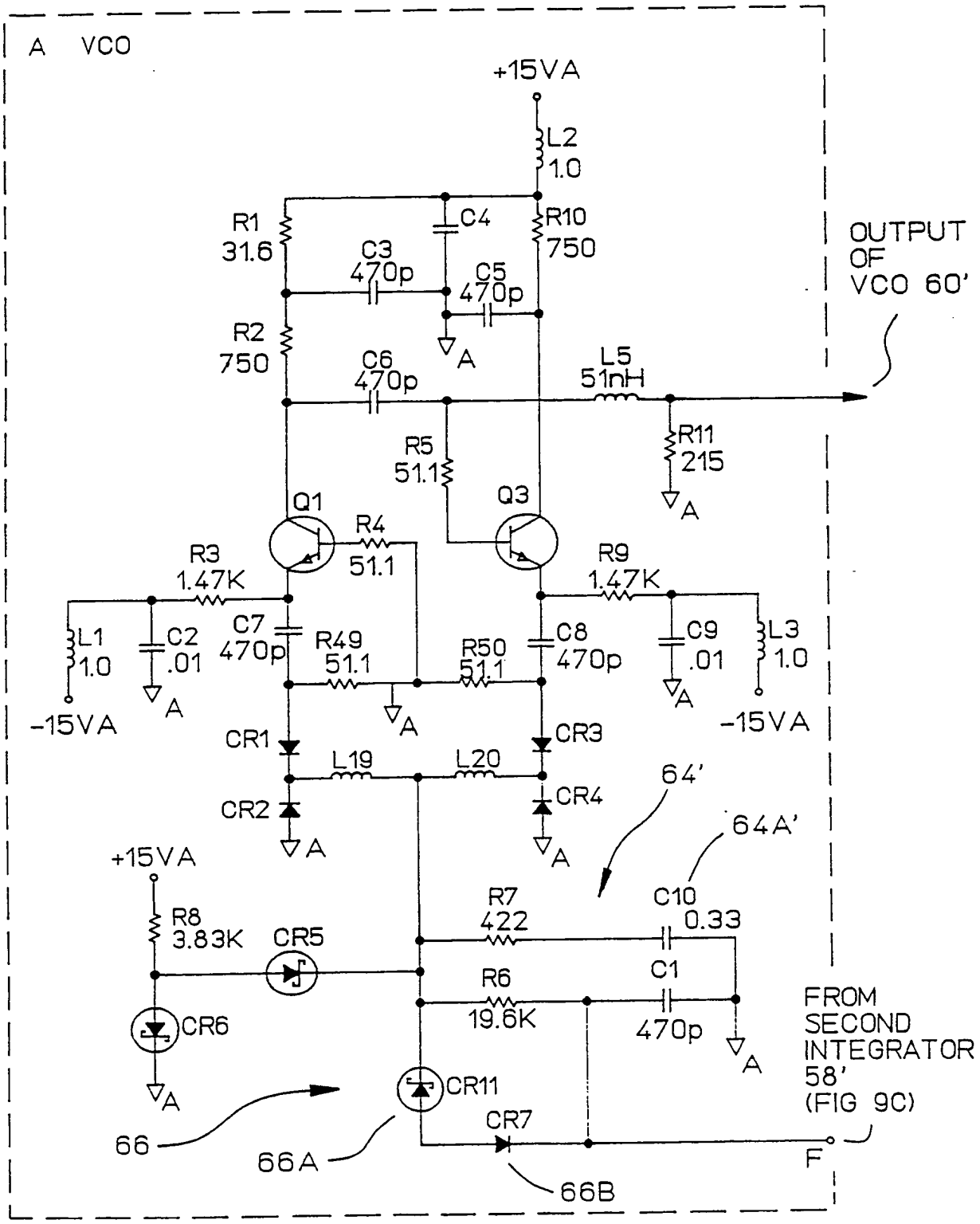

A VCO
+15VA
L2
1.0
R1
31.6
C4
R10
750
C3
470p
C5
470p
OUTPUT
OF
VCO 60'
R2
750
A
C6
470p
L5
51nH
R11
215
R5
51.1
Q1
Q3
R4
51.1
R3
1.47K
R9
1.47K
L1
1.0
C2
.01
C7
470p
R49
51.1
R50
51.1
C8
470p
C9
.01
L3
1.0
-15VA
-15VA
CR1
CR3
L19
L20
CR2
CR4
64'
64A'
+15VA
R7
422
C10
0.33
R8
3.83K
CR5
R6
19.6K
C1
470p
FROM
SECOND
INTEGRATOR
58'
(FIG 9C)
CR6
CR11
CR7
66
66A
66B
F

FIG 9D

PHASE-LOCKING CIRCUIT FOR SWEPT SYNTHESIZED SOURCE PREFERABLY HAVING STABILITY ENHANCEMENT CIRCUIT

Background of the Invention

This invention relates to sources for generating high-frequency electrical signals and, more particularly, to frequency synthesizers for generating swept radio-frequency (RF) signals, including signals at microwave frequencies. Specifically, one embodiment of the invention provides a swept synthesized source having a phase-lock loop for providing improved control of the frequencies generated by the swept synthesized source and preferably also provides reduced phase-lock loop acquisition time and improved stability for a low-frequency synthesizer incorporated into the swept synthesized source to yield a swept synthesized source having improved frequency accuracy and reduced phase noise.

A block diagram of a conventional swept synthesized source is shown in Fig. 1. Such a swept synthesized source generates an electrical signal having a selectively variable frequency. Typically, the frequency is varied, or swept, either continuously or in discrete steps from one frequency, known as the "start frequency," to a higher frequency, known as the "stop frequency," the range of frequencies from the start frequency to the stop frequency being known as the "frequency span."

The typical swept synthesized source, generally indicated by the numeral 10 shown in Fig. 1, comprises a microwave electronically tunable oscillator 12, a frequency sampler 14, a low-frequency synthesizer 16, a phase/frequency detector 18, a reference oscillator 20, a loop filter/signal conditioning circuit 22, an electronic pretuning circuit 24, such as a digital-to-analog converter (DAC), and means to open and close the phase lock loop, such as a switch 26. Operation and synchronization

of the low-frequency synthesizer 16, the pretuning circuit 24, and the switch 26 are controlled by a controller 28, such as a microprocessor.

Considered in more detail, in order to lock to any selected start frequency within the operating range of the swept synthesized source 10, the microwave oscillator 12 is pretuned near this frequency with the switch 26 operated by the controller 28 to the dotted line position indicated in Fig. 1, so that the main phase-lock loop of the swept synthesized source is open, and a tuning input of the microwave oscillator is connected to the pretuning circuit 24. Also, the low-frequency synthesizer 16 is set to its lowest frequency by the controller 28.

Once pretuning is complete, the switch 26 is operated to the solid line position indicated in Fig. 1, so that the main phase-lock loop is closed. The selected start frequency is attained when the microwave oscillator 12 locks on to the proper comb tooth that appears in the output of the sampler 14, as is well known. This occurs when the signal produced by the phase/frequency detector 18 reaches a null during operation of the main phase-lock loop after the loop is closed. The low-frequency synthesizer 16 is then swept by the controller 28 up to a frequency which produces the selected stop frequency of the microwave oscillator 12.

In order for the swept synthesized source 10 to be swept from the selected start frequency to the selected stop frequency, the frequency of the low-frequency synthesizer 16 is incremented by the controller 28 as will be described shortly. This causes the signal produced by the phase/frequency detector 18 to deviate from the null condition and feed an error voltage to the tuning input of the microwave oscillator 12, which drives the microwave oscillator to operate at a higher frequency. Once this higher frequency is attained, the main phase-lock loop operates so that the phase/frequency

detector 18 again reaches a null condition. This process is repeated with the frequency being increased, either continuously or in discrete steps, until the selected stop frequency is reached.

The swept synthesized source 10 of the type shown in Fig. 1 has several known limitations. Most importantly, it is imperative to pretune accurately so that the microwave oscillator 12 does not lock on to the wrong comb tooth of the sampler 14.

However, there are inherent problems with the conventional pretuning technique described above. Specifically, the required pretune voltage produced by the pretuning circuit 24 is typically derived from a pretune calibration algorithm. For example, in the case where the pretuning circuit 24 is a DAC, the pretune calibration algorithm is based on a transfer function of selected pretune frequency versus required DAC setting. The voltage produced by the DAC in response to this DAC setting is converted to a current that is fed to the tuning input of the microwave oscillator 12 to drive the microwave oscillator.

Unfortunately, the microwave oscillator 12 is typically a yttrium-iron-garnet (YIG) oscillator or other tunable device comprising magnetic material. Therefore, the microwave oscillator 12 has a hysteresis in its tuning characteristic. This means that a given pretuning current produced in response to the DAC voltage can yield a range of output frequencies dependent on the previous amount of tuning current present.

Also, another difficulty results from the non-linear pretuning curve for the tuning current versus actual pretune frequency transfer function for different frequency bands of the microwave oscillator 12. The conventional swept synthesized source 10 employs a piece-wise linear approximation to this curve, requiring derivation of several segment endpoints during the

pretune calibration. However, this pretune calibration is affected by changes in time and temperature.

Consequently, the accuracy of the swept synthesized source 10 in generating a selected pretune frequency can be relatively low due to the hysteresis characteristic of the microwave oscillator 12. Additionally, the repeatability with which the swept synthesized source 10 can generate that selected pretune frequency is significantly affected over changes in time and temperature. Therefore, a swept synthesized source is needed to overcome these limitations.

Additionally, the low-frequency synthesizer 16 can comprise a synthesizer having a conventional configuration shown in the block diagram of Fig. 2. As shown in Fig. 2, a phase-lock loop for the low-frequency synthesizer 16 typically comprises another reference oscillator 52, another phase/frequency detector 54, integrator(s) 56, 58, a voltage controlled oscillator (VCO) 60, and a frequency divider 62. The VCO 60 is phase-locked to the reference oscillator 52 by using the phase-lock loop for the low-frequency synthesizer 16. The frequency of the VCO 60 is N times the frequency of the reference oscillator 52, where N is the divide number of the frequency divider 62 set by the controller 28.

In order to minimize phase error in high-speed frequency tracking, maximum gain is desired in the phase-lock loop for the low-frequency synthesizer 16. This can be achieved by using two integrators 56 and 58, rather than one. A phase-lock loop with two integrators, such as integrators 56 and 58, is conventionally known as a type III loop.

The transient response of the type III phase-lock loop shown in Fig. 2 is determined by the location of the poles and zeros in the loop bandwidth. For a type III phase-lock loop (two integrators 56 and 58), typically each integrator has a pole at 0 Hz and a zero somewhere

between one-half and one-tenth of the loop bandwidth. These zeros are the dominant elements in determining overall transient response characteristics of the type III phase-lock loop.

For example, a type III phase-lock loop with a loop bandwidth of 100 kHz could have two integrators 56 and 58, each with a pole at 0 Hz and a zero at 10 kHz. This would result in a type III phase-lock loop with minimal ringing and overshoot for large changes in the divide number N and, hence, large changes in the frequency of the VCO 60.

In order to enhance phase-noise performance in a type III phase-lock loop, one conventional technique is to include a passive lag-lead network 64 between the second integrator 58 and a tune voltage input of the VCO 60, as shown in Fig. 2. In the given example, the second integrator 58 would still have its pole frequency at 0 Hz, but would shift the zero down to a low frequency, such as 25 Hz. The lag-lead network 64 would have a pole at this same frequency to cancel the zero and a zero at the original circuit location (in the above example, 10 kHz). The overall response of the second integrator 58 and the lag-lead network 64 would be equivalent (a pole at 0 Hz and a zero at 10 kHz), but any broadband noise at the output of the second integrator would be greatly attenuated by the lag-lead network. The result is improved phase-noise performance.

Transient response and/or stability of the phase-lock loop for the low-frequency synthesizer 16 are major design considerations. The phase-lock loop must settle quickly when the divide number N is changed to sweep the frequency of the low-frequency synthesizer 16 and, hence, the frequency of the microwave oscillator 12 shown in Fig. 1. The greatest demand is placed on the phase-lock loop of the low-frequency synthesizer 16 when the change in N is large.

Now, the stability of the phase-lock loop for the low-frequency synthesizer 16 can be divided into two components: small-signal stability and large-signal stability. Small-signal stability is defined as the transient response to small changes to N, with the resulting transient control voltages within the phase-lock loop of the low-frequency synthesizer 16 less than their saturation limits. Large-signal stability is defined as the response to large changes in N, with the integrators 56 and 58 entering into their saturation region. Under this large-signal operating condition, the operation of the phase-lock loop of the low-frequency synthesizer 16 is no longer linear.

A major limitation of the conventional low-frequency synthesizer 16 shown in Fig. 2 is its large-signal transient response. With a cutoff frequency of 25 Hz, the slew time during large changes in N is considerable. In order to discharge a capacitor 64A of the lag-lead network 64, the second integrator 58 swings to its negative rail, with the first integrator 56 at its positive rail. As the first integrator 56 recovers from saturation, it pulls the second integrator 58 out of saturation also. However, there is a lag time between the change in the output voltage of the first integrator 56 in response to the change in the output of the second integrator 58, as well as the output of the lag-lead network 64. This lag time creates a phase shift in the type III phase-lock loop, which results in instability. This instability appears as ringing in the transient response of the low-frequency synthesizer 16 at best, or as oscillation at worst.

Considered in more detail, Fig. 3 illustrates the transient response of the low-frequency synthesizer 16 shown in Fig. 2 during large-signal operation in response to a large change in the divide number N. When the divide number N is altered from a large number to a small

number, the frequency of the VCO 60 switches from a high value to a low value. At the time that N is altered, the output of the first integrator 56 swings positive, the output of the second integrator 58 swings negative, the capacitor 64A of the lag-lead network 64 is discharged, and the frequency of the VCO 60 decreases. As the frequency of the VCO 60 continues to decrease past the desired frequency, the output of the first integrator 56 then goes negative to compensate. However, the time delay between the output of the first integrator 56 and the change in the output of the lag-lead network 64 is too great, introducing excessive phase shift and, hence, instability, as indicated by the arrow shown in Fig. 3.

Sharpe, C.A., "Speed up PLLs," Electronic Design 24, (November 22, 1977) discloses speed-up circuitry to improve phase-lock loop acquisition time. Three approaches are suggested. The first approach is to detect large changes in the divide number N and slew the VCO at a rate faster than normal phase-lock loop dynamics allow by switching between two VCOs operating at different frequencies or range-switching one VCO with capacitors in an associated tank circuit, but the exact frequency shift needed must be known. The second approach is to select circuit values to optimize the slew rate without sacrificing the other phase-lock loop characteristics. The third approach is to tune the VCO frequency coarsely with channel information using a summing network, or with a tuning voltage using varactors, along with frequency lock-in by the phase-lock loop. These approaches are relatively restrictive and complex. In any event, stability of the phase-lock loop is not addressed, and, consequently, stability problems persist.

Therefore, there is a need for a phase-lock loop for a low-frequency synthesizer which has improved acquisition time and stability. It is also desirable to

incorporate such a low-frequency synthesizer into a swept synthesized source to yield a swept synthesized source having improved frequency accuracy and reduced phase noise over a broad range of operating frequencies.

Summary of the Invention

One embodiment of the present invention provides a swept synthesized source preferably comprising a microwave electronically tunable oscillator, a frequency sampler, a low-frequency synthesizer, a phase/frequency detector, a reference oscillator, a loop filter/signal conditioning circuit, an electronic pretuning circuit, such as a digital-to-analog converter (DAC), and means to open and close the phase lock loop, such as a switch. Additionally, in the case where the swept synthesized source is operated across several frequency bands, the swept synthesized source further comprises a track and hold circuit.

In accordance with this embodiment of the invention, the tuning current fed to the microwave oscillator is initially zeroed to eliminate hysteresis effects, for example, by initially disconnecting the tuning input of the microwave oscillator from the remainder of the circuit. Also, the electronic pretuning circuit, such as a DAC, is initially set to produce a voltage to drive the microwave oscillator, so that the microwave oscillator will operate near its minimum operating frequency, and a divide number N is reset, so that the low-frequency synthesizer is initialized near its minimum frequency of operation. Then, the pretuning circuit is connected to the tuning input of the microwave oscillator.

Next, the main phase-lock loop is closed, and the microwave oscillator phase locks to its minimum operating frequency. The low-frequency synthesizer in the main phase-lock loop is then swept to drive the microwave oscillator over the desired frequency span.

If the desired frequency span extends over several frequency bands, the low-frequency synthesizer is swept over its operating frequency range, which in turn sweeps the microwave oscillator to the maximum frequency of the present frequency band. Then, the main phase-lock loop is opened, and the tuning input of the microwave oscillator is connected to the track and hold circuit, so that the frequency of the microwave oscillator is held at the maximum frequency of the present frequency band, and the low-frequency synthesizer is re-initialized. Then, the switch is operated to disconnect the track and hold circuit and again close the main phase-lock loop, and the low-frequency synthesizer is swept again. Each frequency band is crossed in a similar manner until the desired frequency span from a selected start frequency to a selected stop frequency has been swept. The method in accordance with the invention compensates pretuning to eliminate hysteresis, tuning nonlinearity, and drift over time and temperature of the microwave oscillator.

Furthermore, the present invention provides a pretune calibration method so that the microwave oscillator will initially phase-lock to its minimum operating frequency as the swept synthesized source is initialized to begin its sweep. The pretune calibration method uses an internal frequency counter, an internal voltage comparator, and an internal voltmeter.

At the start of pretune calibration in accordance with one embodiment of the method of the invention, the DAC used to pretune the microwave oscillator is set to zero. Then, the minimum tuning voltage is measured. Next, the DAC is set to its maximum value. Thereafter, the maximum available tuning voltage is measured. From these measured values, a slope and offset are derived to allow computing a calibrated DAC value corresponding to each pretuning voltage over the entire range of available pretuning voltages.

An initial DAC "seed" value is stored in read only memory in the controller. This seed value is the DAC number to pretune the microwave oscillator to a frequency which is a predetermined frequency below the desired initial lock-up frequency corresponding to the minimum operating frequency of the microwave oscillator.

The DAC number is set to the seed value, so that the microwave oscillator is initially pretuned using the DAC seed value. Then, the initial frequency of the low-frequency synthesizer is set to near its minimum, and the microwave oscillator is pretuned using the current DAC number, which is initially the seed value. Thereafter, the actual tuning voltage produced by the DAC in response to the seed value is measured and stored.

Next, the main phase-lock loop is closed and phase-lock is attempted. The actual tuning voltage present when the main phase-lock loop is closed is stored. The operation of the main phase-lock loop is monitored by the internal voltage comparator to determine whether or not lock-up occurs.

If phase-lock does not occur, the DAC number is incremented by one. Then, initial phase-lock of the main phase-lock loop is again attempted at a tuning voltage derived from the incremented DAC number.

If lock-up occurs, the actual tuning voltage is measured and compared with the tuning voltage at pretune using the DAC seed value. From these two values (i.e., the actual tuning voltage at which phase-lock occurs and the initial pretune voltage), it is inferred whether the lock-up frequency is above or whether it is below the selected pretune frequency. If the lock-up frequency is below the selected pretune frequency, the DAC number is incremented by one, and phase-lock is again attempted at a tuning voltage derived from the incremented DAC number.

If the swept synthesized source phase locks to a frequency above the selected pretune frequency, it is

determined whether or not the actual phase-lock frequency is the correct frequency (correct harmonic number) corresponding to the minimum operating frequency of the microwave oscillator. At this juncture, the main phase-lock loop is opened. Furthermore, a setting for the DAC number needed to produce the actual phase-lock frequency is derived based on measurement of the actual phase-lock frequency tuning voltage and slope and offset, the DAC is set with this number, and the corresponding pretuning voltage produced by the DAC is used to pretune the microwave oscillator. That is, the microwave oscillator is pretuned to a frequency using the same tuning voltage present when the swept synthesized source initially phase locked.

Next, the frequency output of the sampler is counted by the internal frequency counter and stored. The frequency of the low-frequency synthesizer is then shifted a known amount, and the frequency output of the sampler is again counted and stored.

The difference between the two counted sampler frequencies and the known amount that the frequency of the low-frequency synthesizer shifts are used to determine the harmonic to which the swept synthesized source is tuned. If phase-lock to the correct harmonic has occurred, the DAC number that was earlier derived (i.e., the DAC number corresponding to the tuning voltage which resulted in initial phase-lock) is stored, and this stored DAC number is used for pretuning to produce lock-up at the minimum operating frequency of the microwave oscillator during subsequent operation.

Otherwise, if it is determined that initial lock-up to the correct harmonic has not occurred, the initial pretune DAC number is incremented by one, and phase-lock is again attempted at a tuning voltage derived from the incremented DAC number. Preferably, a predetermined maximum number of attempts is undertaken to phase-lock to

the correct pretune frequency, or the pretune calibration process is aborted.

Additionally, one embodiment of the invention provides a low-frequency synthesizer comprising a type III phase-lock loop incorporating another reference oscillator, another phase/frequency detector, two integrators, a passive lag-lead network, a voltage controlled oscillator (VCO), and a frequency divider. In accordance with the invention, the low-frequency synthesizer additionally comprises a zener diode in the lag-lead network to enable asymmetric charging and discharging of a capacitor in the lag-lead network to maintain loop stability (i.e., to avoid ringing and oscillation) by preventing loop saturation, especially for large changes in the divide number N which determines the operating frequency of the low-frequency synthesizer, thereby enhancing the stability, phase-noise performance, and transient response of the type III phase-lock loop.

The swept synthesized source in accordance with the various embodiments of the invention provides a phase-lock loop to achieve precise control of the frequencies generated by the swept synthesized source. The swept synthesized source also preferably provides improved phase-lock loop acquisition time and stability for a low-frequency synthesizer incorporated into the swept synthesized source to yield a swept synthesized source having improved frequency accuracy and reduced phase noise over a broad range of operating frequencies.

Brief Description of the Drawings

The above and other features of the invention and the concomitant advantages will be better understood and appreciated by persons skilled in the field to which the invention pertains in view of the following description given in conjunction with the accompanying drawings. In the drawings:

Fig. 1 is a block diagram of a conventional swept synthesized source;

Fig. 2 is a block diagram of a conventional low-frequency synthesizer incorporated into the swept synthesized source shown in Fig. 1;

Fig. 3 illustrates the transient response of the conventional low-frequency synthesizer shown in Fig. 2 during large-signal operation in response to a large change in the divide number N;

Fig. 4 is a block diagram of a swept synthesized source in accordance with one embodiment of the invention;

Fig. 5 is a flow chart of one embodiment of the method in accordance with the invention for achieving accurate and repeatable sweeping of the frequency of the swept synthesized source shown in Fig. 4;

Fig. 6, comprising Figs. 6A-6C, is a flow chart of one embodiment of a method in accordance with the invention for pretune calibration of the swept synthesized source shown in Fig. 4;

Fig. 7 is a block diagram of a low-frequency synthesizer in accordance with one embodiment of the invention for incorporation into the swept synthesized source shown in Fig. 4 to enhance the stability, phase-noise performance, and transient response of the swept synthesized source;

Fig. 8, comprising Figs. 8A, 8B, and 8C, illustrates the transient responses of the low-frequency synthesizer shown in Fig. 7; and

Fig. 9, comprising Figs. 9A-9D, are schematic diagrams for implementation of various circuits of the swept synthesized source shown in Fig. 4.

Detailed Description of the Preferred Embodiments

Previously, to lock to any arbitrary frequency within the range of a swept synthesized source, a microwave oscillator was simply pretuned near this frequency. The

required pretune voltage was derived from a pretune calibration algorithm based on a transfer function of pretune frequency to the voltage produced by a digital-to-analog converter (DAC). As each frequency band of a desired swept frequency span was crossed, the main phase-lock loop was opened, and the DAC was set to a new value for the beginning frequency of the succeeding frequency band. Therefore, pretuning has heretofore not compensated for hysteresis and tuning nonlinearity and is susceptible to drift of the microwave oscillator over time and temperature. Consequently, the accuracy and repeatability of the frequency sweep of the swept synthesized source has been less than desirable.

One embodiment of a swept synthesized source for achieving accurate, repeatable swept frequency operation in accordance with the invention, generally indicated by the numeral 10', is shown in Fig. 4. The swept synthesized source 10' comprises a microwave electronically tunable oscillator 12' connected in a main phase-lock loop with a frequency sampler 14', a low-frequency synthesizer 16', a phase/frequency detector 18', a reference oscillator 20', a loop filter/signal conditioning circuit 22', an electronic pretuning circuit 24', such as a digital-to-analog converter (DAC), and means to open and close the loop, such as a switch 26', similar to the configuration of the conventional swept synthesized source 10 shown in Fig. 1. Also similar to the conventional swept synthesized source 10 shown in Fig. 1, the switch 26' has a first position indicated by the solid line position in Fig. 4, in which an output of the loop filter 22' is connected to the tuning input of the microwave oscillator 12', and a second position indicated by the dotted line position in Fig. 4, in which the output of the pretuning circuit 24' is connected to the tuning input of the microwave oscillator.

Still referring to Fig. 4, the swept synthesized source 10' in accordance with one embodiment of the invention further comprises a track and hold circuit 30 having an input connected to the output of the loop filter 22'. The track and hold circuit 30 stores the output of the loop filter 22' shown in Fig. 4, which corresponds to the most current value of the voltage produced during operation of the main phase-lock loop for driving the microwave oscillator 12'.

Also, in accordance with the one embodiment of the swept synthesized source 10' of the invention, the switch 26' has a third position indicated by the dashed line position in Fig. 4, in which the tuning input of the microwave oscillator 12' is disconnected from the remainder of the circuit and, for example, allows a zener diode and a resistor (not shown) connected across a tuning coil (not shown) of the microwave oscillator to turn on so that energy stored in the magnetic field of the coil is dissipated in a circulating current through the coil, zener diode, and resistor. Finally, the switch 26' has a fourth position indicated by the dash-dot line position in Fig. 4, in which the output of the track and hold circuit 30 is connected to the tuning input of the microwave oscillator 12'.

As shown in Fig. 4, operation and synchronization of the pretuning circuit 24' and the switch 26' are controlled by a controller 28', such as a microprocessor. The controller 28' also controls and synchronizes operation of the low-frequency synthesizer 16'.

In accordance with one embodiment of the method of the invention, illustrated in Fig. 5, the swept synthesized source 10' is operated so that the tuning current initially fed to the microwave oscillator 12' is zeroed, as indicated by the numeral 32 shown in Fig. 5. Therefore, any energy stored in the magnetic field resulting from previous operation of the microwave

oscillator 12' is allowed to dissipate so that hysteresis effects are eliminated and, hence, do not affect subsequent operation of the microwave oscillator. Also, as indicated by the numeral 34 shown in Fig. 5, the pretune voltage is initially set to produce a voltage to cause the microwave oscillator 12' to be driven to operate near its minimum operating frequency, and the divide number N is reset so that the low-frequency synthesizer 16 is initialized near its minimum frequency of operation. Then, the pretuning current is fed to the microwave oscillator 12', as indicated by the numeral 36 shown in Fig. 5.

Next, as indicated by the numeral 38 shown in Fig. 5, pretuning is discontinued, and the main phase-lock loop is closed. Consequently, the microwave oscillator 12' phase locks to its minimum operating frequency. Then, the low-frequency synthesizer 16' in the main phase-lock loop is swept to drive the microwave oscillator 12' to in turn sweep the microwave oscillator across a frequency range, including the portion of the range from the minimum frequency to the desired start frequency (if these frequencies are in fact different) and then from the start frequency to the stop frequency, thereby sweeping the desired frequency span, as indicated by the numeral 40 shown in Fig. 5.

If the frequency span to be swept by the swept synthesized source 10' (i.e., the portion of the range from the minimum frequency of the microwave oscillator 12' to the stop frequency) includes all or a portion of a different frequency band(s) of the microwave oscillator than the initial frequency band, as determined by the numeral 42 shown in Fig. 5, the microwave oscillator is swept to the maximum frequency of the present frequency band. The maximum frequency of the current frequency band corresponds to the point in operation where the low-frequency synthesizer 16' is swept to its maximum

frequency (i.e., the maximum value of the divide number N), as indicated by the numeral 44 shown in Fig. 5. At the point in the operating characteristic where the low-frequency synthesizer 16' reaches its maximum frequency for the one frequency band, the main phase-lock loop is opened, and the tuning input of the microwave oscillator 12' is connected to the output of the track and hold circuit 30 so that the frequency of the microwave oscillator is held at the current frequency by the track and hold circuit, as indicated by the numeral 46 shown in Fig. 5. Then, as indicated by the numeral 48 shown in Fig. 5, while the main phase-lock loop is open, the low-frequency synthesizer 16' is re-initialized to near its minimum frequency (the divide by N number is reset to its minimum).

Next, the main phase-lock loop is again closed, as indicated by the numeral 50 shown in Fig. 5. The low-frequency synthesizer 16' is then swept again so that the microwave oscillator 12' resumes sweeping to higher frequencies in the adjacent frequency band, as indicated by the numeral 40 shown in Fig. 5. Each frequency band is crossed in a similar manner until the selected stop frequency is attained, as determined by the numeral 42 shown in Fig. 5.

Considered in more detail with reference to Fig. 4, the swept synthesized source 10' operates as follows to solve problems attributable to hysteresis and non-linearity of the microwave oscillator 12'. In order to assure that a given pretuning current will yield a selected pretune frequency, the tuning current is always set to zero prior to pretuning. This, in effect, removes the stored hysteresis in the magnetic material of the microwave oscillator 12'. Accordingly, the controller 28' operates the switch 26' to the dashed line position indicated in Fig. 4 to zero the tuning current to the microwave oscillator 12'. Therefore, the tuning input of

the microwave oscillator 12' is first disconnected from the remainder of the circuit before the microwave oscillator is pretuned.

When the tuning current is effectively reset to zero by disconnecting the tuning input of the microwave oscillator 12' from the remainder of the circuit, a finite amount of time is required for the magnetic field in the magnetic material of the microwave oscillator to dissipate (i.e., for the microwave oscillator to stabilize). This time can be on the order of tens of milliseconds, for example, approximately 30 milliseconds in the case that the main coil of the microwave oscillator 12' incorporates a 1 henry coil.

Furthermore, the microwave oscillator 12' is consistently pretuned to near its minimum frequency when it is pretuned. In order to pretune the microwave oscillator 12' to near the minimum frequency of its operating frequency range, the controller 28' sets the DAC of the pretuning circuit 24' with a value that will cause the DAC to produce a voltage needed to provide the tuning current required to pretune the microwave oscillator to near its minimum operating frequency. Then, the controller 28' operates the switch 26' to the dotted line position indicated in Fig. 4 to connect the output of the pretuning circuit 24' to the tuning input of the microwave oscillator 12' to drive the microwave oscillator to operate near its minimum operating frequency.

In order to phase lock the microwave oscillator 12' to a selected pretune frequency, the time for the microwave oscillator to settle is proportional to the extent of the frequency range over which the microwave oscillator must slew to the selected pretune frequency. The higher the pretune frequency, the longer the settling time is for the microwave oscillator 12'. Pretuning to the minimum frequency of operation of the microwave oscillator 12' in

accordance with the invention minimizes the settling time of the microwave oscillator, as well as causes the operation of the microwave oscillator to be more repeatable.

Next, the main phase-lock loop is closed. In order to close the main phase-lock loop, the controller 28' operates the switch 26' to its solid line position indicated in Fig. 4 to connect the output of the loop filter 22' to the tuning input of the microwave oscillator 12'. The operation of the main phase-lock loop subsequently causes the microwave oscillator 12' to lock to its minimum operating frequency.

The low-frequency synthesizer 16' is then swept up to a frequency which produces the stop frequency of the swept synthesized source 10' or to the maximum frequency of the low-frequency synthesizer, which ever occurs first. If the selected stop frequency of the swept synthesized source 10' is in another frequency band of the microwave oscillator 12' (that is, a different comb tooth at the output of the sampler 14'), the controller 28' sweeps the microwave oscillator to the maximum frequency of the present frequency band by sweeping the low-frequency synthesizer 16' to its maximum frequency (i.e., to the maximum divide number N). The controller 28' then operates the switch 26' to the dash-dot line position indicated in Fig. 4 so that the output of the track and hold circuit 30 is connected to the tuning input of the microwave oscillator 12'. Consequently, the microwave oscillator 12' is held at the current frequency by the track and hold circuit 30.

Operation of the switch 26' to its dash-dot line position indicated in Fig. 4 also opens the main phase-lock loop so that the controller 28' can re-initialize the low-frequency synthesizer 16' to near its minimum operating frequency by resetting the divide number N to its minimum. Re-initialization of the low-frequency

synthesizer 16' is needed to initiate sweeping of the next frequency band of the range of operation of the microwave oscillator 12'.

Then, the controller 28' operates the switch 26' to the solid line position indicated in Fig. 4 to disconnect the tuning input of the microwave oscillator 12' from the output of the track and hold circuit 30 and again close the main phase-lock loop. Since the microwave oscillator 12' was held on the comb tooth of the sampler 14' at the completion of the previous sweep of the low-frequency synthesizer 16', operation continues from this operating point. Thereafter, when the controller 28' again causes the low-frequency synthesizer 16' to sweep from its minimum toward its maximum frequency, the microwave oscillator 12' will move from its lock on the comb tooth at the highest frequency of the previous frequency band and track the low-frequency synthesizer to generate higher frequencies. Each frequency band is crossed in a similar manner until the selected stop frequency of the swept synthesized source 10' is attained.

The above-described operation minimizes the influence of the hysteresis, tuning nonlinearity, and time and temperature drift of the microwave oscillator 12'. The basis of the solution in accordance with the embodiment of the swept synthesized source 10' shown in Fig. 4 is to eliminate hysteresis problems by always resetting the tuning current to zero before pretuning the microwave oscillator 12'. Furthermore, the microwave oscillator 12' is restricted to be pretuned to near its minimum operating frequency and is always driven to its minimum operating frequency to avoid pretuning the microwave oscillator to any arbitrary frequency. This eliminates the need to derive piece-wise linear transfer function segments used to compute arbitrary pretune frequencies for crossing different frequency bands during operation of the swept synthesized source 10'. Nonlinearity of the

microwave oscillator 12' is likewise not a major concern, as long as it does not contain any discontinuities.

Also in accordance with the present invention, a pretune calibration method is provided to assure proper initial pretuning of the swept synthesized source 10'. This pretune calibration method is preferably performed prior to the step 32 shown in Fig. 5. One embodiment of the pretune calibration method in accordance with the invention for the swept synthesized source 10' is shown in the flow chart of Figs. 6A-6C and will now be described.

The purpose of the pretune calibration method is to derive the DAC value, or number, needed to pretune the microwave oscillator 12' to approximately the initial lock-up frequency (i.e., the minimum operating frequency of the microwave oscillator). Once pretuned near this frequency, the main phase-lock loop of the swept synthesized source 10' is closed, and phase-lock is achieved. It is necessary that the pretune frequency approximately equal the initial lock-up frequency in order to avoid phase-locking to the wrong comb tooth of the sampler 14'.

The pretune calibration method shown in Figs. 6A-6C uses an internal frequency counter 15 connected to the output of the sampler 14', an internal voltage comparator 19 connected to the output of the phase/frequency detector 18', and an internal voltmeter 25 connected to the tuning input of the microwave oscillator 12', as shown in Fig. 4. The internal voltmeter 25 is used to measure the tuning voltage fed to the microwave oscillator 12'. In the embodiment of the swept synthesized source 10' shown in Fig. 4, the internal frequency counter 15 has a maximum frequency limitation of approximately 18 MHz, so the frequency of the swept synthesized source cannot be counted directly. Consequently, the internal frequency counter 15 is used

to count the intermediate frequency from the output of the sampler 14'. This frequency is:

$$Fif = N * Fn.f - Fs$$

where: Fif = the intermediate frequency;

N = harmonic comb tooth number;

Fn.f = frequency of the low-frequency (e.g., fractional-n) synthesizer 16'; and

Fs = frequency of the microwave oscillator 12'.

Pretune calibration is preferably performed when the swept synthesized source 10' is powered-up, on source preset, and whenever the pretune frequency has varied more than approximately 30 MHz from the previously derived value. (After each sweep, the DAC pretune number is adjusted for an optimum offset from the desired initial lock-up frequency.)

Referring to Figs. 6A-6C, at the start of pretune calibration, the DAC is set to its minimum value (e.g., zero), as indicated by the numeral 72 shown in Fig. 6A. Then, as indicated by the numeral 74 shown in Fig. 6A, the resulting minimum tuning voltage, Vmin, is measured. Next, the DAC is set to its maximum value, as indicated by the numeral 76 shown in Fig. 6A. Thereafter, as indicated by the numeral 78 shown in Fig. 6A, the resulting maximum available tuning voltage, Vmax, is measured. From these values for Vmin and Vmax, a slope and offset are derived to allow computing a calibrated DAC value corresponding to each pretuning voltage over the entire range of available pretuning voltages, as indicated by the numeral 80 shown in Fig. 6A.

An initial DAC "seed" value is stored in read only memory (EEPROM) in the controller 28' at the factory. This seed value is the DAC number which is set at the factory to pretune the microwave oscillator 12' to a frequency approximately 50 MHz below the desired initial lock-up frequency corresponding to the minimum operating frequency of the microwave oscillator. This large offset

(50 MHz) is predetermined so that the initial pretune frequency will always be below the desired initial lock-up frequency irrespective of worst-case temperature conditions and any aging effects experienced by the microwave oscillator 12'.

As indicated by the numeral 82 shown in Fig. 6A, the DAC number is initially set to the seed value, so that the microwave oscillator 12' is initially pretuned using the DAC seed value, and "loop_counter" is set to zero. Then, the divide number N is set near its minimum to determine the initial frequency of the low-frequency synthesizer 16', and the microwave oscillator 12' is pretuned using the current DAC number, which is initially the seed value, as indicated by the numeral 84 shown in Fig. 6A. Thereafter, the actual tuning voltage produced by the DAC in response to the seed value is measured and stored as "pret_volt", as indicated by the numeral 86 shown in Fig. 6A.

Next, as indicated by the numeral 88 shown in Fig. 6A, the main phase-lock loop is closed, and phase-lock is attempted. The actual tuning voltage present when the main phase-lock loop is closed is stored as "start_lock_volt", as indicated by the numeral 90 shown in Fig. 6A.

The operation of the main phase-lock loop is monitored to determine whether or not lock-up occurs, as indicated by the numeral 92 shown in Fig. 6B. For example, the output of the phase/frequency detector 18' is checked by the internal voltage comparator 19 shown in Fig. 4 to test whether or not phase-lock has been achieved.

If phase-lock does not occur, the DAC number is incremented by one, and "loop_counter" is also incremented by one, as indicated by the numeral 94 shown in Fig. 6C. If "loop_counter" exceeds twenty (i.e., twenty previous attempts have failed to effect initial lock-up), as indicated by the numeral 96 shown in Fig.

6C, the pretune calibration process is terminated, as indicated by the numeral 98 shown in Fig. 6C. Otherwise, initial phase-lock of the main phase-lock loop is again attempted, as indicated by the steps 84, 86, 88, 90, and 92 shown in Figs. 6A and 6B, at a tuning voltage derived from the incremented DAC number.

If lock-up occurs, as determined at the step 92 shown in Fig. 6B, the actual tuning voltage is measured and compared with the tuning voltage at pretune. From these two values (i.e., the actual tuning voltage at which phase-lock occurs and the initial pretune voltage), it is inferred whether the lock-up frequency is above or whether it is below the selected pretune frequency, as indicated by the numeral 100 shown in Fig. 6B. If the lock-up frequency is below the selected pretune frequency, the DAC number is incremented by one, as indicated by the numeral 94 shown in Fig. 6C, and phase-lock is again attempted, as indicated by the steps 84, 86, 88, 90, and 92 shown in Figs. 6A and 6B, at a tuning voltage derived from the incremented DAC number. Again, however, as indicated by the steps 96 and 98 shown in Fig. 6C, a maximum of twenty attempts is undertaken to phase lock to the correct start frequency.

If the swept synthesized source 10' phase locks to a frequency above the selected pretune frequency, it is determined whether or not the actual phase-lock frequency is the correct frequency (correct harmonic number) corresponding to the minimum operating frequency of the microwave oscillator 12'. At this juncture, the main phase-lock loop is opened, as indicated by the numeral 102 shown in Fig. 6B. Furthermore, a setting for the DAC number needed to produce the actual phase-lock frequency is derived based on measurement of the actual phase-lock frequency tuning voltage (start_lock_volt) and slope and offset values determined at the step 80 shown in Fig. 6A, the DAC is set with this number, and the corresponding

pretuning voltage produced by the DAC is used to pretune the microwave oscillator 12', as indicated by the numeral 104 shown in Fig. 6B. That is, the microwave oscillator 12' is pretuned to a frequency using the same tuning voltage as when the swept synthesized source 10' was initially phase-locked.

Next, the frequency output of the sampler 14' (Fif) is counted and stored as "first_freq", as indicated by the numeral 106 shown in Fig. 6B. As indicated by the numeral 108 shown in Fig. 6B, the frequency of the low-frequency synthesizer 16' is then shifted a known amount, and the frequency output of the sampler 14' is again counted and stored as "second_freq", as indicated by the numeral 110 shown in Fig. 6B.

Since the microwave oscillator 12' is not phase-locked, its frequency will drift by a discernible amount. It is important to shift the low-frequency synthesizer 16' as far as possible to achieve a maximum shift in the frequency output of the sampler 14'. This minimizes the effect of the drift of the microwave oscillator 12'.

Initially, for example, the swept synthesized source 10' can be approximately 12 MHz below the harmonic of the low-frequency synthesizer 16'. After the frequency shift of the low-frequency synthesizer 16' occurs, the swept synthesized source 10' can be approximately 12 MHz above the harmonic of the low-frequency synthesizer. This yields a frequency shift of approximately 24 MHz, while remaining well below the maximum frequency limitation of 18 MHz of the internal frequency counter 15 at the output of the sampler 14'. (Drift of the microwave oscillator 12' will decrease the approximately 6 MHz margin and, hence, the choice of 12 MHz for the example).

The difference between the two counted sampler frequencies and the known amount that the frequency of the low-frequency synthesizer 16' shifts are used to determine the harmonic to which the swept synthesized

source 10' is tuned, as indicated by the numeral 112 shown in Fig. 6B. If phase-lock to the correct harmonic has occurred, as determined by the numeral 114 shown in Fig. 6B, the DAC number derived at the step 104 shown in Fig. 6B is stored, as indicated by the numeral 116, and this stored DAC number is used for pretuning to produce lock-up at the minimum operating frequency of the microwave oscillator 12' during subsequent operation. This completes the pretune calibration process, as indicated by the numeral 118 shown in Fig. 6B.

Otherwise, if it is determined at the step 114 shown in Fig. 6B that initial lock-up to the correct harmonic has not occurred, the DAC number is incremented by one, as indicated by the step 94 shown in Fig. 6C, and phase-lock is again attempted, as indicated by the steps 84, 86, 88, 90, and 92 shown in Figs. 6A and 6B, at a tuning voltage derived from the incremented DAC number. Again, however, as indicated by the steps 96 and 98 shown in Fig. 6C, a maximum of twenty attempts is undertaken to phase lock to the correct pretune frequency, or the pretune calibration process is aborted.

This invention also addresses the requirement of maintaining phase-lock loop linearity for large changes in the divide number N during operation of the low-frequency synthesizer 16'. One embodiment of the phase-lock loop stability enhancement circuit in accordance with the invention allows a non-linear override during periods of large-signal response of the phase-lock loop of the low-frequency synthesizer 16', but produces no effect during normal small-signal operation, as will now be described with reference to Fig. 7.

As shown in Fig. 7, one embodiment the low-frequency synthesizer 16' in accordance with the invention can comprise another reference oscillator 52', another phase/frequency detector 54', integrator(s) 56' and 58', a voltage controlled oscillator (VCO) 60', a frequency

divider 62', and a lag-lead network 64', comprising a capacitor 64A', connected in a type III phase-lock loop. The VCO 60' is phase-locked to the reference oscillator 52' by using the phase-lock loop. The frequency of the VCO 60' is N times the frequency of the reference oscillator 52', where N is the divide number of the frequency divider 62' set by the controller 28' shown in Fig. 4.

In the embodiment of the low-frequency synthesizer 16' shown in Fig. 7, a phase-lock loop stability enhancement circuit 66 is incorporated to provide a non-linear override during periods of large-signal response of the phase-lock loop of the low-frequency synthesizer 16' but produces no effect during normal small-signal operation. Preferably, the phase-lock loop stability enhancement circuit 66 comprises a normally reverse-biased series-connected zener diode 66A and diode 66B connected across the lag-lead network 64', as shown in Fig. 7.

In order to minimize phase error in high-speed frequency tracking between the low-frequency synthesizer 16' and the microwave oscillator 12' shown in Fig. 4, maximum gain is desired in the phase-lock loop for the low-frequency synthesizer. This can be achieved by using the two integrators 56' and 58'.

The phase-lock loop of the low-frequency synthesizer 16' must settle quickly when the divide number N is changed to sweep the frequency of the low-frequency synthesizer and, hence, the frequency of the microwave oscillator 12' shown in Fig. 4. The resulting transient response voltages within the phase-lock loop are below their saturation limits when changes to N are small and, consequently, the loop exhibits stable small-signal operation. However, in response to large changes to N, the integrators 56' and 58' enter into their saturation region so that in the low-frequency synthesizer 16' there is a potential for large-signal instability.

The large-signal transient response of the low-frequency synthesizer 16' shown in Fig. 7 is as follows. With a cutoff frequency of 25 Hz, for example, the slew time during large changes in the divide number N is considerable. When the divide number N is altered from a large number to a small number, the frequency of the VCO 60' switches from a high value to a low value. At the time that N is altered, the output of the first integrator 56' swings positive, the output of the second integrator 58' swings negative, the capacitor 64A' of the lag-lead network 64' is discharged, and the frequency of the VCO 60' decreases.

As the frequency of the VCO 60' continues to decrease past the desired frequency, the output of the first integrator 56' then swings negative to compensate. However, the time delay between the output of the first integrator 56' and the change in the output of the lag-lead network 64' are potentially too great, introducing excessive phase shift and, hence, potential instability.

The embodiment of the phase-lock loop stability enhancement circuit 66 in accordance with the invention operates as follows. During periods of large-signal switching, the breakdown voltage of the zener diode 66A is exceeded, and the zener diode turns on so that the phase-lock loop stability enhancement circuit 66 overrides the lag-lead network 64' to allow the lag-lead capacitor 64A' to discharge very quickly. As a result, the voltage across the lag-lead network 64' undershoots, causing the input voltage to the lag-lead network to compensate by going positive. The phase-lock loop of the low-frequency synthesizer 16' then overshoots, but the lag-lead capacitor 64A' is charged at a very low charge rate.

Basically, the phase-lock loop stability enhancement circuit 66 allows an asymmetric charging and discharging of the lag-lead capacitor 64A' to improve the retrace

condition. Retrace is defined as the switching from a high frequency of the VCO 60' to a low frequency.

Fig. 8A illustrates the output of the second integrator 58' in the phase-lock loop of the low-frequency synthesizer 16' with the phase-lock loop stability enhancement circuit 66. Note that the settling time is approximately 1.6 milliseconds versus approximately 6 milliseconds shown in Fig. 3 for the phase-lock loop without the phase-lock loop stability enhancement circuit 66. The output voltage of the second integrator 58' remains saturated at its negative rail voltage for several milliseconds, with the loop now in its nonlinear state. Its negative voltage swing is about -8 volts, which is well above the saturation limit. When the phase-lock loop of the low-frequency synthesizer 16' finally recovers from saturation, it overshoots and rings until attaining its final target value.

Fig. 8B illustrates the tune voltage to the VCO 60' (output of the lag-lead network 64') with the phase-lock loop stability enhancement circuit 66. Note that there are several cycles of under- and overshoot before the voltage stabilizes. The undershoot quickly discharges the lag-lead capacitor 64A', while the overshoot voltage has minimal charging effect. This can be seen in Fig. 8C. The change in capacitor voltage versus time is very steep during the discharge period, while the slope is almost flat during the charging period. This cycling repeats until the voltage across the lag-lead capacitor 64A' (and, hence, the output voltage of the lag-lead network 64') converges to the target value. What appears as instability at first glance is actually quite stable on closer inspection. The turn-on voltage of the zener diode 66A determines the hysteresis of the phase-lock loop of the low-frequency synthesizer 16'.

The phase-lock loop stability enhancement circuit 66 greatly improves phase-lock loop transient response time.

When used with a type III phase-lock loop with lag-lead network 64' to improve VCO phase noise, it minimizes loop instability (ringing and oscillation) by preventing loop saturation.

The embodiment of the swept synthesized source 10' shown in Fig. 4, including the low-frequency synthesizer 16' having the phase-lock loop stability enhancement circuit 66 shown in Fig. 7, can be implemented through modifications to a commercially available Model HP 8720B network analyzer available from Hewlett-Packard Company, Palo Alto, California. In the Model HP 8720B, the low-frequency synthesizer 16' is a fractional-n synthesizer. The needed modifications to the circuit of the Model HP 8720B are shown in the schematic circuit diagrams of Figs. 9A-9D. Specifically, Fig. 9A shows an implementation of the loop filter/signal conditioning circuit 22' comprising a "1st INTEGRATOR" and a "2nd INTEGRATOR." The switch 26' preferably incorporates the added circuit which appears at the output of the 1st INTEGRATOR. The values of the components which comprise the 2nd INTEGRATOR in the Model HP 8720B have also been modified to the values shown in Fig. 9A, which facilitates implementation of the added track and hold circuit 30. Finally, the values of the components which comprise the "YIG 1 MAIN COIL DRIVER," "YIG 2 MAIN COIL DRIVER," and "FM COIL DRIVER" of the microwave oscillator 12' have also been modified to the values shown in Fig. 9A from the values of the components in the Model HP 8720B. As shown in Fig. 9B, the phase/frequency detector 54' is modified from that in the Model HP 8720B to provide detection of bidirectional, as opposed to only unidirectional, shifts in the frequency output of the sampler 14'. Fig. 9C shows the second integrator 58' added to the circuit of the Model HP 8720B at the output of the integrator resident in the previous circuit. Finally, Fig. 9D shows the lag-lead network/phase-lock

loop stability enhancement circuit 64', 66 added to the circuit of the Model HP 8720B between the added second integrator 58' and the VCO resident in the previous circuit. The internal frequency counter 15, internal voltage comparator 19, and internal voltmeter 25 shown in Fig. 4 are presently resident in the circuit of the Model HP 8720B.

Finally, Appendices A-D comprise a source code listing of the firmware executed by the controller 28'. Appendix A is the firmware which controls phase locking of the swept synthesized source 10'. Appendix B is the firmware which controls the DAC of the pretuning circuit 24'. Appendix C is the firmware for controlling operation of the low-frequency synthesizer 16'. Finally, Appendix D is the firmware for the pretune calibration method in accordance with the embodiment of the invention shown in Figs. 6A-6C.

Accordingly, the present invention provides a low-frequency synthesizer which has improved transient response and stability of the phase-lock loop of the low-frequency synthesizer. It also provides a low-frequency synthesizer for a swept synthesized source to yield a swept synthesized source having improved frequency accuracy and reduced phase noise over a broad range of operating frequencies.

The foregoing description is offered primarily for purposes of illustration. While a variety of embodiments of a swept synthesized source has been disclosed, it will be readily apparent to those skilled in the art that numerous other modifications and variations not mentioned above can still be made without departing from the spirit and scope of the invention as claimed below.

WHAT IS CLAIMED IS:

1. A swept synthesized source comprising:

tunable oscillator means having a tuning input and an output;

low-frequency synthesizer means having a control input and an output;

frequency sampler means having a first input connected to the output of the tunable oscillator means, a second input connected to the output of the low-frequency synthesizer means, and an output;

reference oscillator means having an output;

phase detector means having a first input connected to the output of the frequency sampler means, a second input connected to the output of the reference oscillator means, and an output;

signal conditioning means having an input connected to the output of the phase detector means and an output;

electronic pretuning means having a control input and an output;

switching means having a control input, an output connected to the tuning input of the tunable oscillator means, and at least three positions, including a first position in which the tuning input of the tunable oscillator means is connected to the output of the signal conditioning means, a second position in which the tuning input of the tunable oscillator means is connected to the output of the electronic pretuning means and a third position in which there is no connection to the tuning input of the tunable oscillator means; and

controller means connected to the control inputs of the low-frequency synthesizer means, electronic pretuning means, and switching means for generating control signals;

the controller means initially providing a control signal to operate the switching means to the

third position so that energy stored in the tunable oscillator means is dissipated;

whereby hysteresis effects in the operation of the tunable oscillator means are eliminated.

2. The swept synthesized source of claim 1 wherein the electronic pretuning means comprises a digital-to-analog converter (DAC).

3. The swept synthesized source of claim 1 wherein the swept synthesized source is operated across a plurality of frequency bands, the swept synthesized source further comprising a track and hold circuit having an input connected to the output of the signal conditioning means and an output, and wherein the switching means has at least a fourth position in which the tuning input of the tunable oscillator means is connected to the output of the track and hold circuit when a maximum frequency of a frequency band is reached in response to a control signal from the controller means.

4. The swept synthesized source of claim 1, further comprising a frequency counter connected to the output of the frequency sampler means, a voltage comparator connected to the output of the phase detector means, and a voltmeter connected to the tuning input of the tunable oscillator means.

5. The swept synthesized source of claim 1 wherein the low-frequency synthesizer means comprises:

a voltage controlled oscillator (VCO) having a tune input and an output, the output of the VCO being connected to the second input of the frequency sampler means;

frequency divider means having a control input connected to the controller means, an input connected to the output of the VCO, and an output;

second reference oscillator means having an output;

second phase detector means having a first input connected to the output of the second reference oscillator means, a second input connected to the output of the frequency divider means, and an output;

first integrator means having an input connected to the output of the second phase detector means and an output; and

second integrator means having an input connected to the output of the first integrator means and an output coupled to the tune input of the VCO.

6. The swept synthesized source of claim 5 wherein the low-frequency synthesizer means further comprises a passive lag-lead network having an input connected to the output of the second integrator means and an output connected to the tune input of the VCO for coupling the second integrator means to the VCO, whereby phase-lock loop acquisition time is reduced.

7. The swept synthesized source of claim 6 wherein the low-frequency synthesizer means further comprises a phase-lock loop stability enhancement circuit connected between the input and the output of the lag-lead network.

8. The swept synthesized source of claim 7 wherein the lag-lead network comprises a resistor connected between the output of the second integrator means and the tune input of the VCO and a capacitor coupled between the input of the VCO and common and wherein the phase-lock loop stability enhancement circuit comprises a reverse-biased zener diode connected between the output of the second integrator means and the tune input of the VCO to control charging and discharging of the capacitor during large-signal operation.

9. In a low-frequency synthesizer comprising a voltage controlled oscillator (VCO) having a tune input and an output; frequency divider means having a control input, an input connected to the output of the VCO, and an output; reference oscillator means having an output;

phase detector means having a first input connected to the output of the reference oscillator means, a second input connected to the output of the frequency divider means, and an output; first integrator means having an input connected to the output of the phase detector means and an output; second integrator means having an input connected to the output of the first integrator means and an output; a passive lag-lead network having an input connected to the output of the second integrator means and an output connected to the tune input of the VCO; and controller means connected to the control input of the frequency divider means; the improvement comprising:

a phase-lock loop stability enhancement circuit connected between the input and the output of the lag-lead network.

10. The low frequency synthesizerof claim 9 wherein the lag-lead network comprises a resistor connected between the output of the second integrator means and the tune input of the VCO and a capacitor coupled between the input of the VCO and common and wherein the phase-lock loop stability enhancement circuit comprises a reverse-biased zener diode connected between the output of the second integrator means and the tune input of the VCO to control charging and discharging of the capacitor during large-signal operation.

11. A swept synthesized source comprising:

tunable oscillator means having a tuning input and an output;

low-frequency synthesizer means having a control input and an output, the low-frequency synthesizer means comprising:

a voltage controlled oscillator (VCO) having a tune input and an output; frequency divider means having a control input, an input connected to the output of the VCO, and an output; first reference oscillator means having an output;

first phase detector means having a first input connected to the output of the reference oscillator means, a second input connected to the output of the frequency divider means, and an output; first integrator means having an input connected to the output of the first phase detector means and an output; second integrator means having an input connected to the output of the first integrator means and an output; a passive lag-lead network having an input connected to the output of the second integrator means and an output connected to the tune input of the VCO, and a phase-lock loop stability enhancement circuit connected between the input and the output of the lag-lead network;

frequency sampler means having a first input connected to the output of the tunable oscillator means, a second input connected to the output of the VCO of the low-frequency synthesizer means, and an output;

second reference oscillator means having an output;

second phase detector means having a first input connected to the output of the frequency sampler means, a second input connected to the output of the second reference oscillator means, and an output;

signal conditioning means having an input connected to the output of the second phase detector means and an output;

electronic pretuning means having a control input and an output;

switching means having a control input, an output connected to the tuning input of the tunable oscillator means, and at least three positions, including a first position in which the tuning input of the tunable oscillator means is connected to the

output of the signal conditioning means, a second position in which the tuning input of the tunable oscillator means is connected to the output of the electronic pretuning means and a third position in which there is no connection to the tuning input of the tunable oscillator means; and

controller means connected to the control inputs of the frequency divider means of the low-frequency synthesizer means, electronic pretuning means, and switching means for generating control signals;

the controller means initially providing a control signal to operate the switching means to the third position so that energy stored in the tunable oscillator means is dissipated;

whereby hysteresis effects in the operation of the tunable oscillator means are eliminated.

12. The swept synthesized source of claim 11 wherein the swept synthesized source is operated across a plurality of frequency bands, the swept synthesized source further comprising a track and hold circuit having an input connected to the output of the signal conditioning means and an output, and wherein the switching means has at least a fourth position in which the tuning input of the tunable oscillator means is connected to the output of the track and hold circuit when a maximum frequency of a frequency band is reached in response to a control signal from the controller means.

13. A method of operating a swept synthesized source, comprising the steps of:

initially zeroing the tuning current fed to a tunable oscillator means included in the swept synthesized source to eliminate hysteresis effects by initially disconnecting a tuning input of the tunable

oscillator means from means for driving the tunable oscillator means;

initially setting electronic pretuning means to produce a voltage to drive the tunable oscillator means so that the tunable oscillator means will operate near its minimum operating frequency;

resetting a divide number N so that a low-frequency synthesizer means is initialized near its minimum frequency of operation;

connecting the electronic pretuning means to the tuning input of the tunable oscillator means;

disconnecting the electronic pretuning means from the tuning input of the tunable oscillator means;

closing a main phase-lock loop so that the tunable oscillator means phase locks to its minimum operating frequency; and

sweeping the low-frequency synthesizer means in the main phase-lock loop to drive the tunable oscillator means over a desired frequency span.

14. The method of claim 13 wherein the desired frequency span extends over a plurality of frequency bands, further comprising the steps of:

sweeping the low-frequency synthesizer means over its operating frequency range to in turn sweep the tunable oscillator means to a maximum frequency of a present frequency band;

opening the main phase-lock loop;

connecting the tuning input of the tunable oscillator means to a track and hold circuit so that the frequency of the tunable oscillator means is held at the maximum frequency of the present frequency band;

re-initializing the low-frequency synthesizer means;

disconnecting the track and hold circuit;

again closing the main phase-lock loop; and

sweeping the low-frequency synthesizer means again.

15. The swept synthesized source of claim 11 wherein the lag-lead network comprises a resistor connected between the output of the second integrator means and the tune input of the VCO and a capacitor coupled between the input of the VCO and common and wherein the phase-lock loop stability enhancement circuit comprises a reverse-biased zener diode connected between the output of the second integrator means and the tune input of the VCO to control charging and discharging of the capacitor during large-signal operation.

16. A pretune calibration method for determining a pretuning signal so that a tunable oscillator means incorporated into a swept synthesized source will initially phase-lock to its minimum operating frequency as the swept synthesized source is initialized to begin its sweep, comprising the steps of:

a) setting electronic pretuning means for the tunable oscillator means to a minimum value;

b) measuring a minimum tuning voltage in response to setting the electronic pretuning means to the minimum value;

c) setting the electronic pretuning means for the tunable oscillator means to a maximum value;

d) measuring a maximum tuning voltage in response to setting the electronic pretuning means to the maximum value;

e) deriving a slope and offset from the measured minimum and maximum values to allow computing calibrated values corresponding to each pretuning voltage over a given range of available pretuning voltages;

f) providing an initial seed value representative of a setting of the electronic pretuning means to pretune the tunable oscillator means to a frequency which is a predetermined frequency below a desired initial phase-lock frequency corresponding to the minimum operating

frequency of the tunable oscillator means;

g) setting the electronic pretuning means with the seed value so that the tunable oscillator means is initially pretuned using the seed value;

h) initializing the frequency of a low-frequency synthesizer means incorporated into the swept synthesized source to near its minimum frequency of operation;

i) connecting the electronic pretuning means to a tuning input of the tunable oscillator means for pretuning the tunable oscillator means;

j) measuring an actual tuning voltage produced by the electronic pretuning means;

k) storing the measured actual tuning voltage produced by the electronic pretuning means;

l) disconnecting the electronic pretuning means from the tuning input of the tunable oscillator means;

m) closing a main phase-lock loop for attempting phase-lock of the tunable oscillator means;

n) measuring an actual tuning voltage present at the tuning input of the tunable oscillator means when the main phase-lock loop is closed;

o) storing the measured actual tuning voltage present at the tuning input of the tunable oscillator means when the main phase-lock loop is closed;

p) monitoring operation of the main phase-lock loop to determine if phase-lock occurs;

q) incrementing the value used to set the electronic pretuning means so that the tunable oscillator means is subsequently pretuned using the incremented value if phase-lock does not occur at step p);

r) repeating steps h) through p) if the value used to set the electronic pretuning means is incremented at step q);

s) measuring an actual tuning voltage at which phase-lock occurs and comparing this actual tuning

voltage with the tuning voltage at pretune using the present value used to set the electronic pretuning means if phase-lock occurs at step p);

t) determining the relationship of the phase-lock frequency to the selected pretune frequency from the two values compared at step s);

u) incrementing the value used to set the electronic pretuning means and repeating steps h) through t) if the phase-lock frequency is determined to be below the selected pretune frequency at step t);

v) determining if the actual phase-lock frequency corresponds to the minimum operating frequency of the tunable oscillator means if the phase-lock frequency is above the selected pretune frequency;

w) storing the present value used to set the electronic pretuning means corresponding to the tuning voltage which resulted in initial phase-lock if phase-lock to the correct harmonic is determined to have occurred at step v) for use in pretuning to produce phase-lock at the minimum operating frequency of the tunable oscillator means during subsequent operation; and

x) incrementing the value used to set the electronic pretuning means and repeating steps h) through w) if it is determined at step v) that phase-lock to the correct harmonic has not occurred.

17. The pretune calibration method of claim 16, wherein step v) comprises:

1) opening the main phase-lock loop;

2) deriving a value used to set the electronic pretuning means needed to produce the actual phase-lock frequency based on measurement of the actual phase-lock frequency tuning voltage and slope and offset;

3) setting the electronic pretuning means with the value derived at step 2) and using a corresponding pretuning voltage produced by the electronic pretuning

means to pretune the tunable oscillator means;

4) counting and storing a first frequency output of a frequency sampler means;

5) shifting a frequency of the low-frequency synthesizer means connected to the frequency sampler means a known amount;

6) counting and storing a second frequency output of the frequency sampler means;

7) computing a difference between the first and second frequency outputs determined at steps 4) and 6), respectively; and

8) using the difference computed at step 7) and the known amount that the frequency of the low-frequency synthesizer means shifts to determine the harmonic to which the tunable oscillator means is tuned.

18. A method of operating a swept synthesized source, comprising the steps of:

a) setting electronic pretuning means for tunable oscillator means incorporated into the swept synthesized source to a minimum value;

b) measuring a minimum tuning voltage in response to setting the electronic pretuning means to the minimum value;

c) setting the electronic pretuning means for the tunable oscillator means to a maximum value;

d) measuring a maximum tuning voltage in response to setting the electronic pretuning means to the maximum value;

e) deriving a slope and offset from the measured minimum and maximum values to allow computing calibrated values corresponding to each pretuning voltage over a given range of available pretuning voltages;

f) providing an initial seed value representative of a setting of the electronic pretuning means to pretune the tunable oscillator means to a frequency which is a

predetermined frequency below a desired initial phase-lock frequency corresponding to the minimum operating frequency of the tunable oscillator means;

g) setting the electronic pretuning means with the seed value so that the tunable oscillator means is initially pretuned using the seed value;

h) initializing the frequency of a low-frequency synthesizer means incorporated into the swept synthesized source to near its minimum frequency of operation;

i) connecting the electronic pretuning means to a tuning input of the tunable oscillator means for pretuning the tunable oscillator means;

j) measuring an actual tuning voltage produced by the electronic pretuning means;

k) storing the measured actual tuning voltage produced by the electronic pretuning means;

l) disconnecting the electronic pretuning means from the tuning input of the tunable oscillator means;

m) closing a main phase-lock loop for attempting phase-lock of the tunable oscillator means;

n) measuring an actual tuning voltage present at the tuning input of the tunable oscillator means when the main phase-lock loop is closed;

o) storing the measured actual tuning voltage present at the tuning input of the tunable oscillator means when the main phase-lock loop is closed;

p) monitoring operation of the main phase-lock loop to determine if phase-lock occurs;

q) incrementing the value used to set the electronic pretuning means so that the tunable oscillator means is subsequently pretuned using the incremented value if phase-lock does not occur at step p);

r) repeating steps h) through p) if the value used to set the electronic pretuning means is incremented at step q);

s) measuring an actual tuning voltage at which phase-lock occurs and comparing this actual tuning voltage with the tuning voltage at pretune using the present value used to set the electronic pretuning means if phase-lock occurs at step p);

t) determining the relationship of the phase-lock frequency to the selected pretune frequency from the two values compared at step s);

u) incrementing the value used to set the electronic pretuning means and repeating steps h) through t) if the phase-lock frequency is determined to be below the selected pretune frequency at step t);

v) determining if the actual phase-lock frequency corresponds to the minimum operating frequency of the tunable oscillator means if the phase-lock frequency is above the selected pretune frequency;

w) storing the present value used to set the electronic pretuning means corresponding to the tuning voltage which resulted in initial phase-lock if the phase-lock to the correct harmonic is determined to have occurred at step v) for use in pretuning to produce phase-lock at the minimum operating frequency of the tunable oscillator means during subsequent operation;

x) incrementing the value used to set the electronic pretuning means and repeating steps h) through w) if it is determined at step v) that phase-lock to the correct harmonic has not occurred;

y) initially zeroing the tuning current fed to the tunable oscillator means included in the swept synthesized source to eliminate hysteresis effects by initially disconnecting a tuning input of the tunable oscillator means from means for driving the tunable oscillator means;

z) initially setting the electronic pretuning means to produce a voltage to drive the tunable oscillator

means so that the tunable oscillator means will operate near its minimum operating frequency;

aa) resetting a divide number N so that the low-frequency synthesizer means is initialised near its minimum frequency of operation;

bb) connecting the electronic pretuning means to the tuning input of the tunable oscillator means;

cc) disconnecting the electronic pretuning means from the tuning input of the tunable oscillator means;

dd) closing the main phase-lock loop so that the tunable oscillator means phase locks to its minimum operating frequency; and

ee) sweeping the low-frequency synthesizer means in the main phase-lock loop to drive the tunable oscillator means over a desired frequency span.

19. The method of claim 18 wherein the desired frequency span extends over a plurality of frequency bands, further comprising the steps of:

sweeping the low-frequency synthesizer means over its operating frequency range to in turn sweep the tunable oscillator means to a maximum frequency of a present frequency band;

opening the main phase-lock loop;

connecting the tuning input of the tunable oscillator means to a track and hold circuit so that the frequency of the tunable oscillator means is held at the maximum frequency of the present frequency band;

re-initializing the low-frequency synthesizer means;

disconnecting the track and hold circuit;

again closing the main phase-lock loop; and

sweeping the low-frequency synthesizer means again.

20. The pretune calibration method of claim 18, wherein step v) comprises:

1) opening the main phase-lock loop;

2) deriving a value used to set the electronic

pretuning means needed to produce the actual phase-lock frequency based on measurement of the actual phase-lock frequency tuning voltage and slope and offset;

3) setting the electronic pretuning means with the value derived at step 2) and using a corresponding pretuning voltage produced by the electronic pretuning means to pretune the tunable oscillator means;

4) counting and storing a first frequency output of a frequency sampler means;

5) shifting a frequency of the low-frequency synthesizer means connected to the frequency sampler means a known amount;

6) counting and storing a second frequency output of the frequency sampler means;

7) computing a difference between the first and second frequency outputs determined at steps 4) and 6), respectively; and

8) using the difference computed at step 7) and the known amount that the frequency of the low-frequency synthesizer means shifts to determine the harmonic to which the tunable oscillator means is tuned.

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Databases (see over)

(i) UK Patent Office

(ii) ONLINE DATABASES : WPI, EDOC

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Documents considered relevant following a search in respect of claims

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	GB 2228380 A - see figure 2	
A	GB 2218869 A - see figures 1, 3	1

Category	Identity of document and relevant passages	Relevant to claim(s)

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